Welcome To

ISSCC 2014
SESSION 18
Biomedical Systems for Improved Quality of Life

A 1V 3mA 2.4GHz Wireless Digital Audio Communication SoC for Hearing-Aid Applications in 0.18µm CMOS

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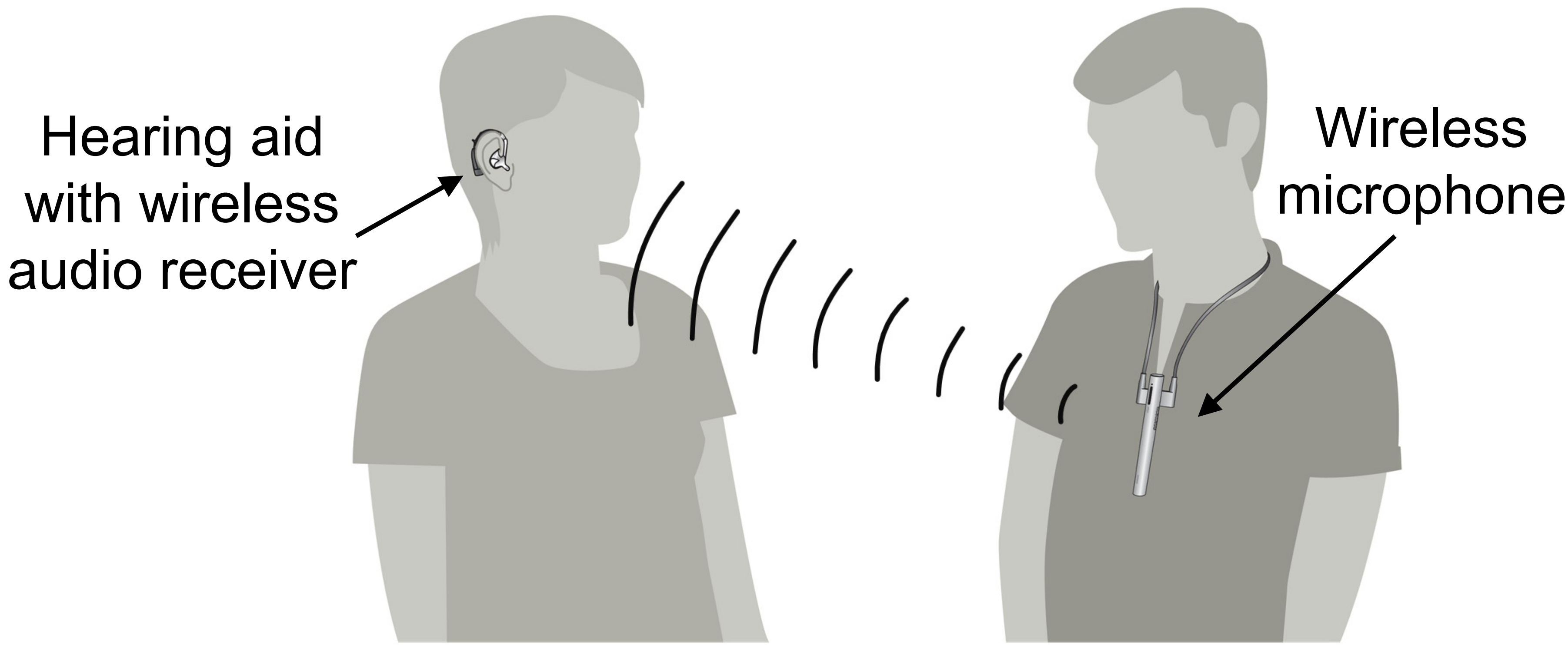
[3]ASICentrum, Prague, Czech Republic

Motivation

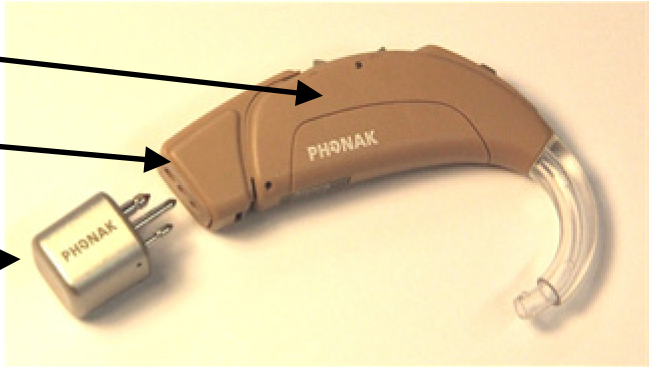
- Improving speech understanding in noise and over distance for persons with hearing loss



Wireless receivers types

- Integrated in hearing aid

- Module connected via the Direct Audio Input (DAI) “Europlug” interface

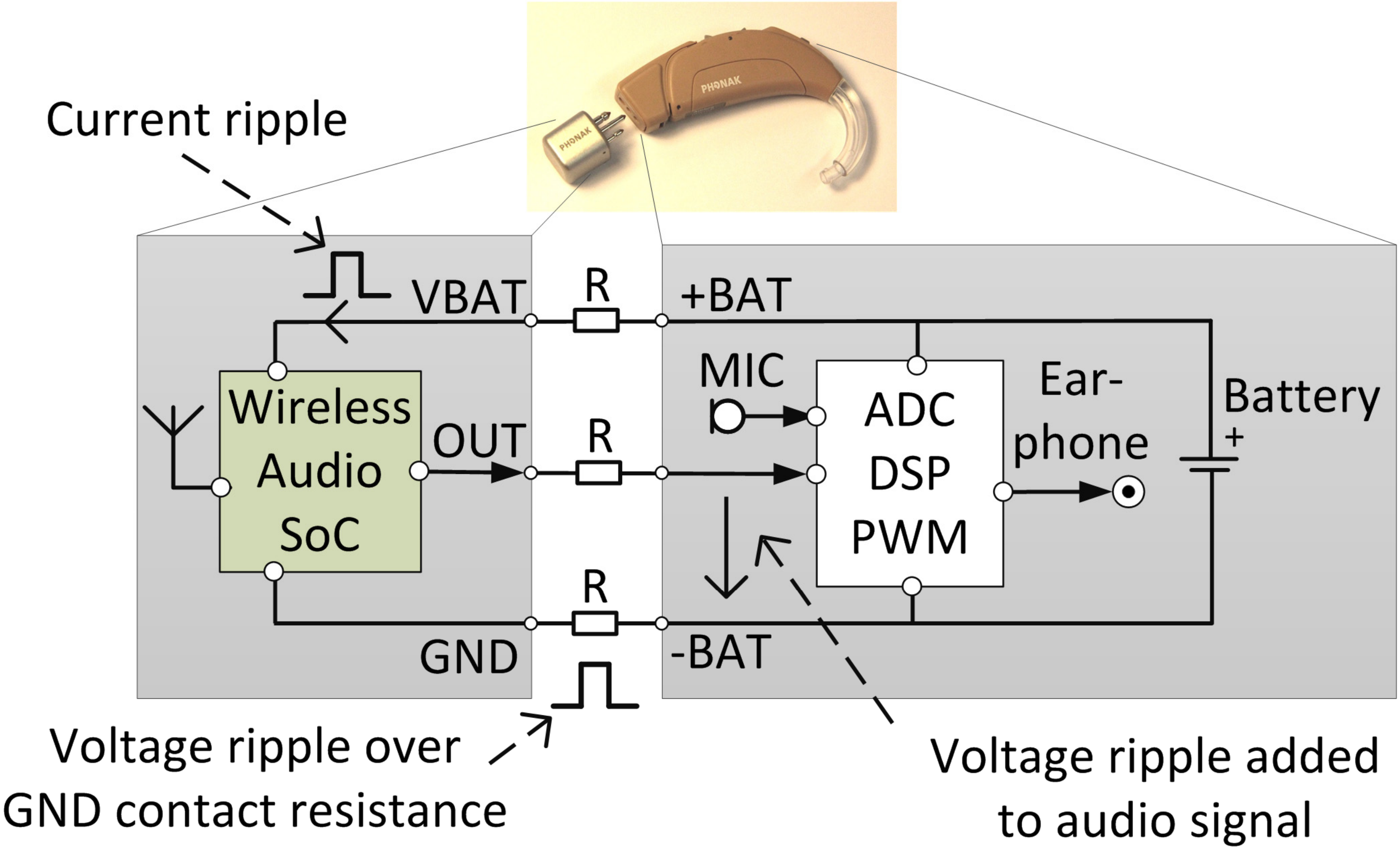


DAI Interface - Applications

- Wired solutions (several vendors)
  – Microphones
  – Cables toward audio output of music player, television, etc.

- Wireless solutions (several vendors)
  – 200 MHz FM receivers
  – 868 MHz and 2.4 GHz digital receivers

DAI Interface - Constraints



Impact of current ripples

1) Voltage ripple across DAI GND contact resistance ➔ Audio signal ripple
   - Audio signal amplitude: 2-10 mV
   - Contact resistance up to 2 Ohms
   - Allowed audio signal voltage ripple < 10 μV

2) VBAT voltage ripple across battery internal resistance, problematic for
   - Hearing aid analog microphone input
   - Hearing aid PWM output
   - Reset threshold

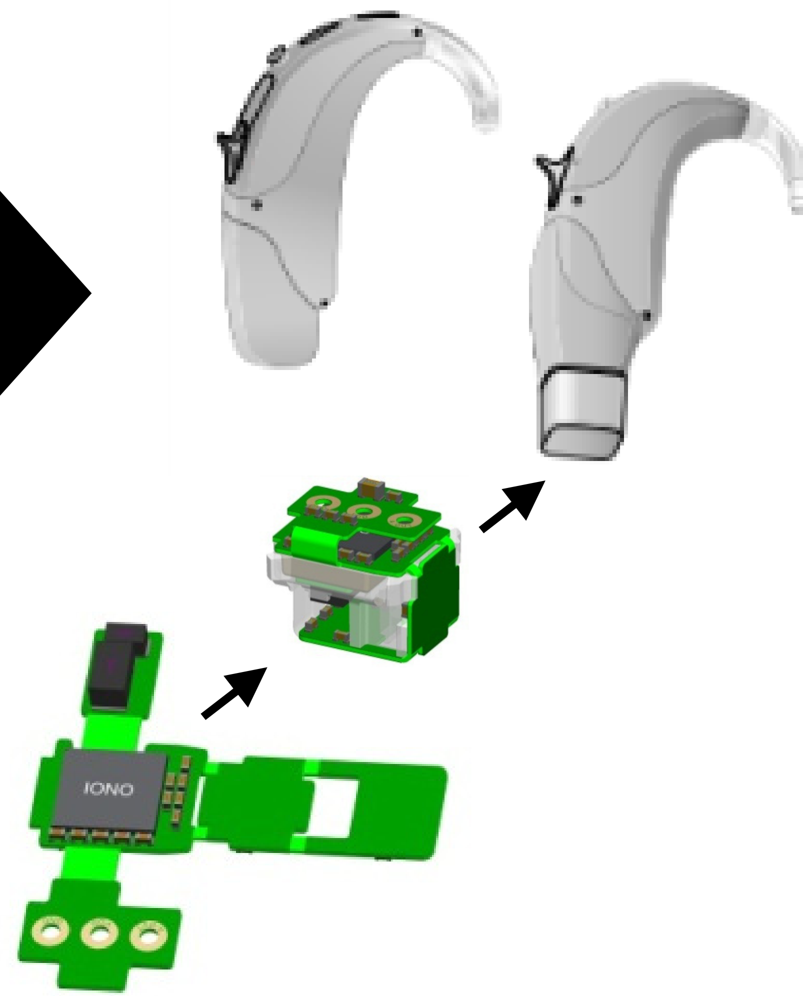
Summary of constraints

- ZincAir battery supply
  - Supply voltage: 1V … 1.4V
  - Average current: < 3 mA
- Analog audio interface with common GND
  - No audible variation of consumed current
- User
  - Audio bandwidth: > 7 kHz
  - Audio delay: < 20 ms
  - Small size

System Overview

Wireless Microphones

Receivers



Digital System @ 2.4 GHz

Benefits:

- Audio quality, privacy
- Usage simplicity (no frequency planning)
- World wide operation

But

Interference & robust & low delay & broadcast

Low Power

Frequency Hopping & Packet repetitions

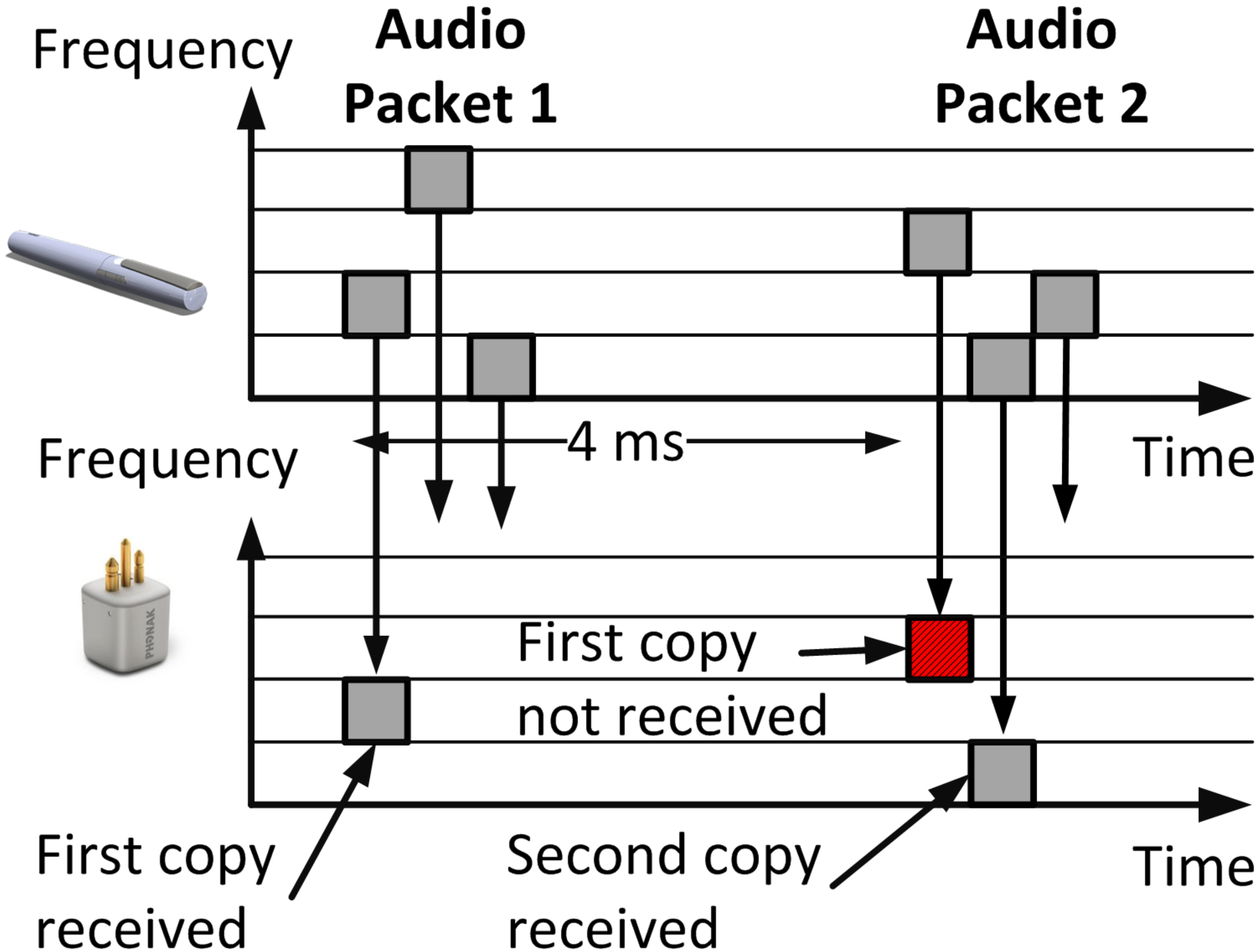
High data rate & Low duty cycle

Pulsed radio current consumption

Communication Protocol Overview

- Radio: 2.4 GHz, GFSK, 2 Mbps
- Protocol:
  - Master/slave star topology
  - Packet radio
  - TDMA (10 slots of 400 us)
  - Adaptive Frequency Hopping (40 channels)
  - Unconditional audio packets repetition

Unconditional audio packets repetitions



Benefits:
- Interference robustness
- Broadcast
- Low power
- Low delay

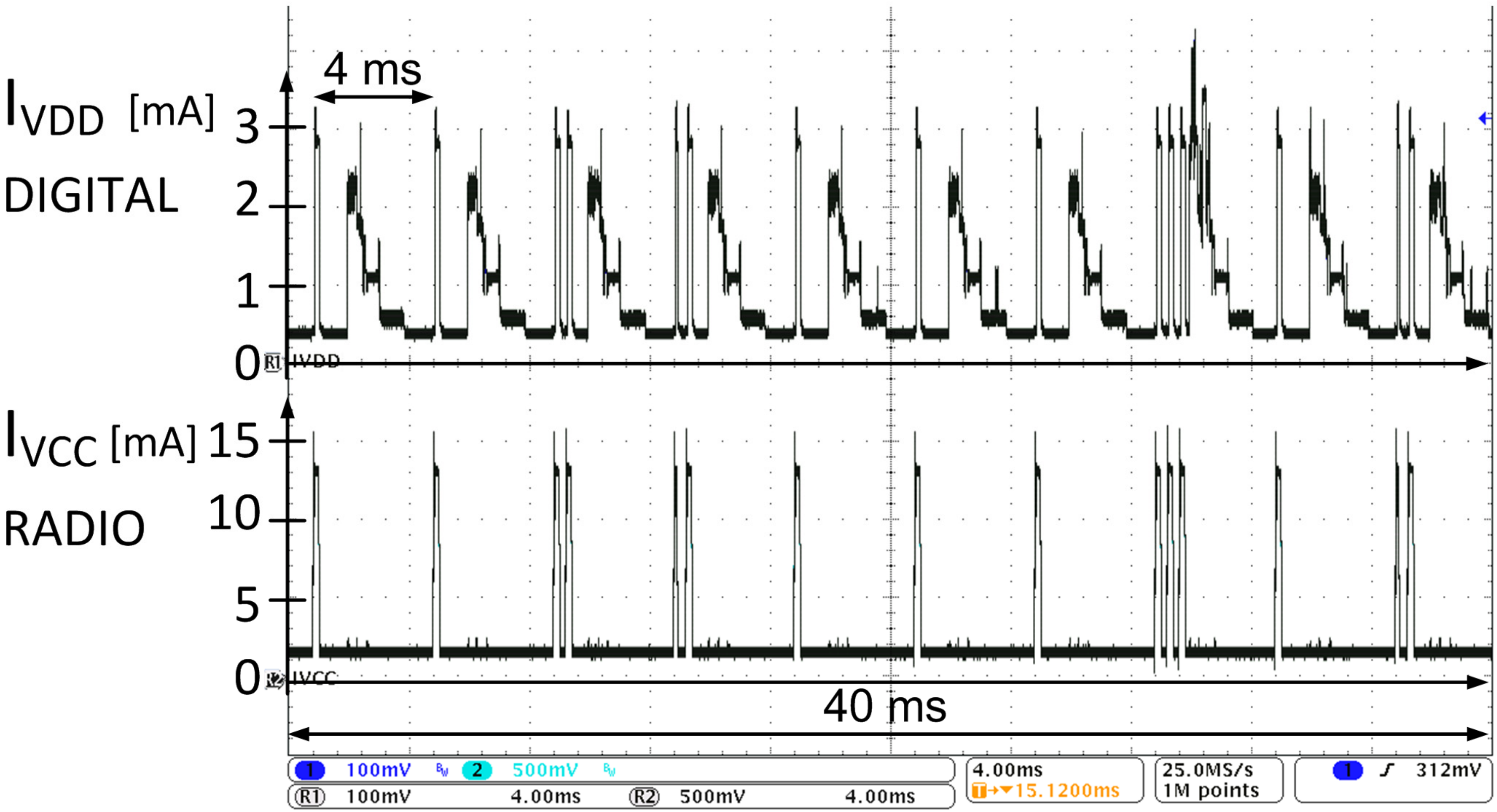
See US2012310394A1, Amre El-Hoiydi

Current consumption variation types

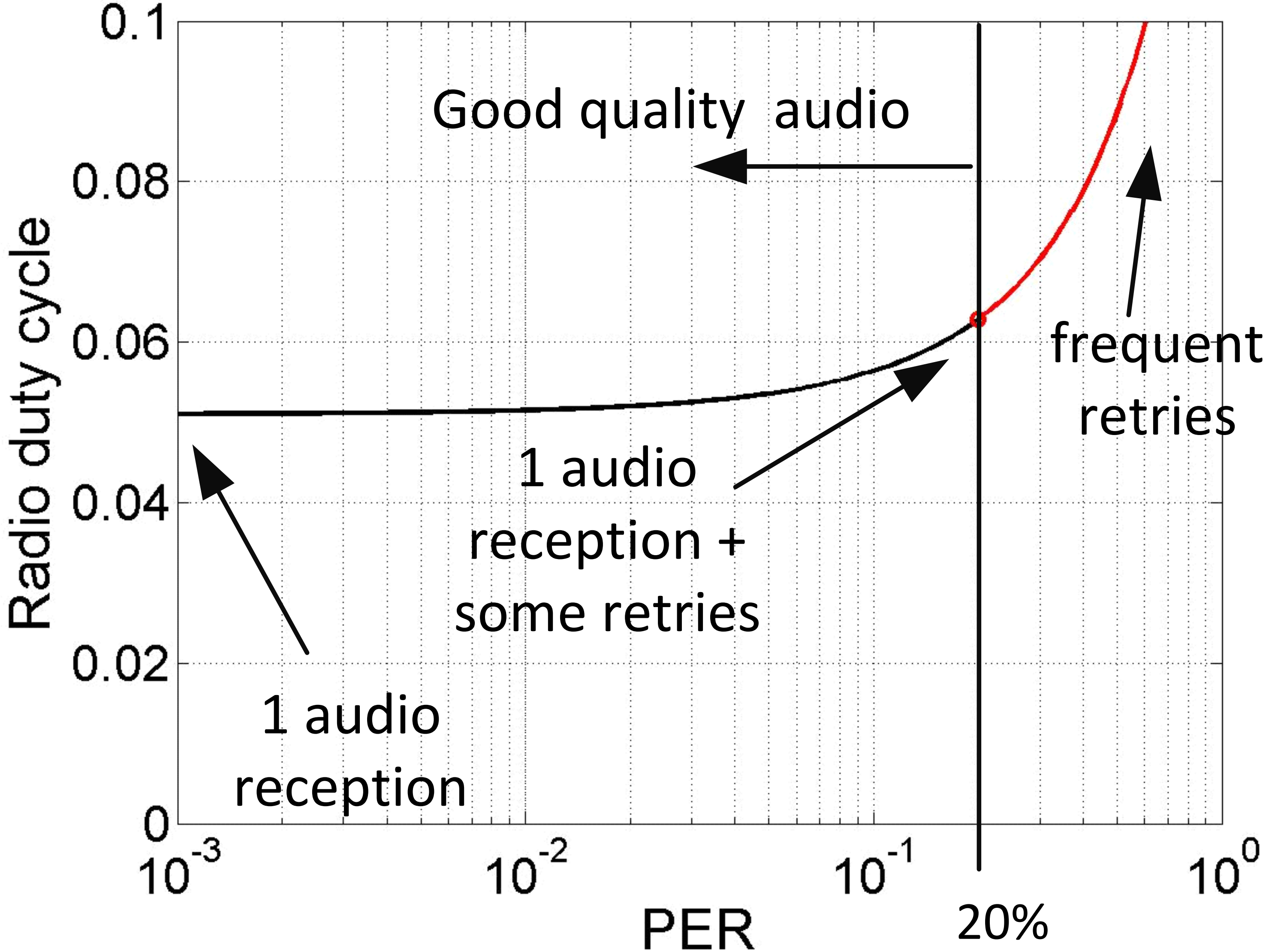
- Fast variations due to TDMA schedule (4 ms period)

- Slow variations due to
  - Change in average PER
  - Sporadic activities (e.g. remote control)

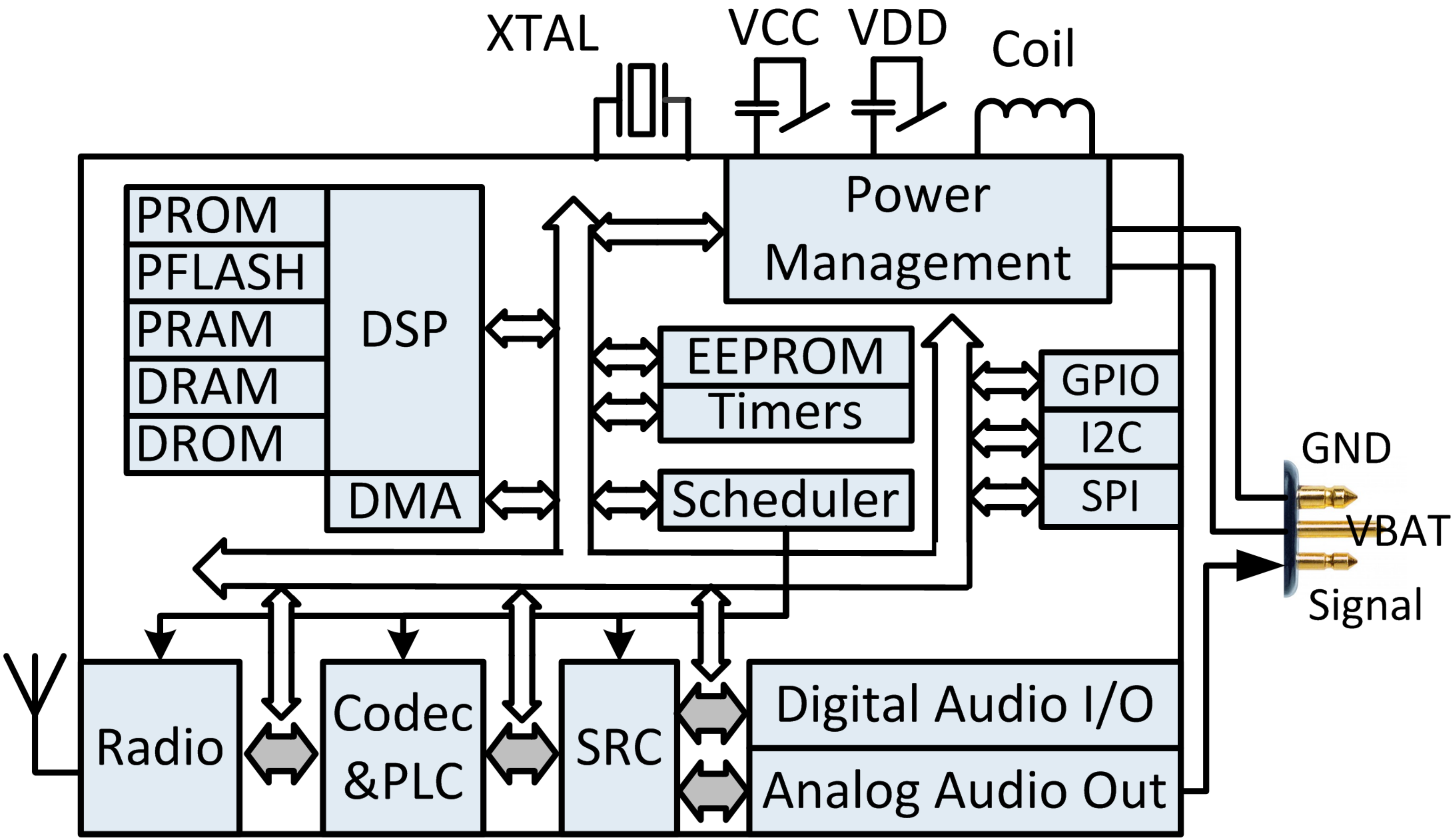
Radio and digital current consumption



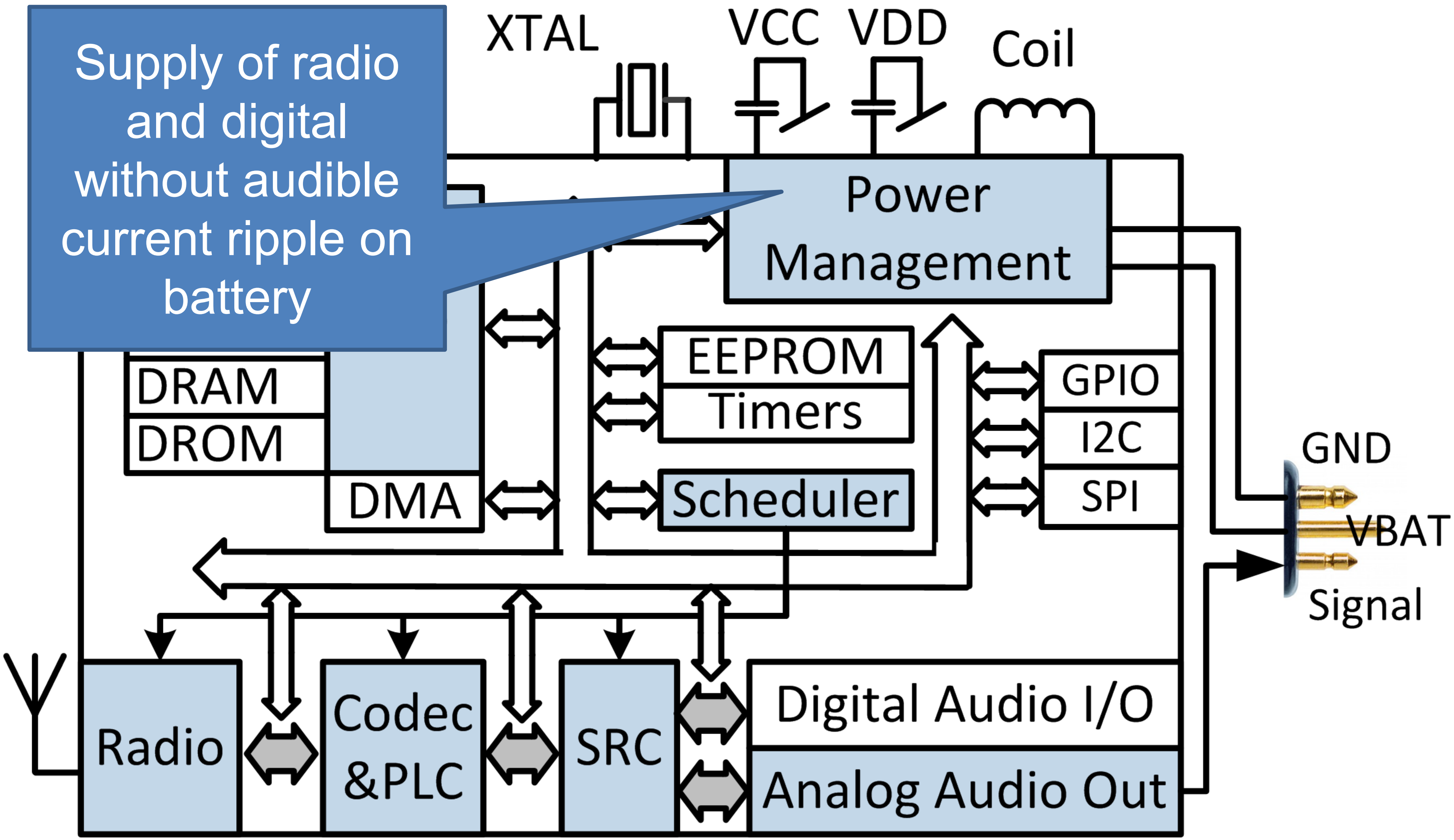
Radio duty cycle versus PER



Wireless Audio SoC Block Diagram



Wireless Audio SoC Block Diagram



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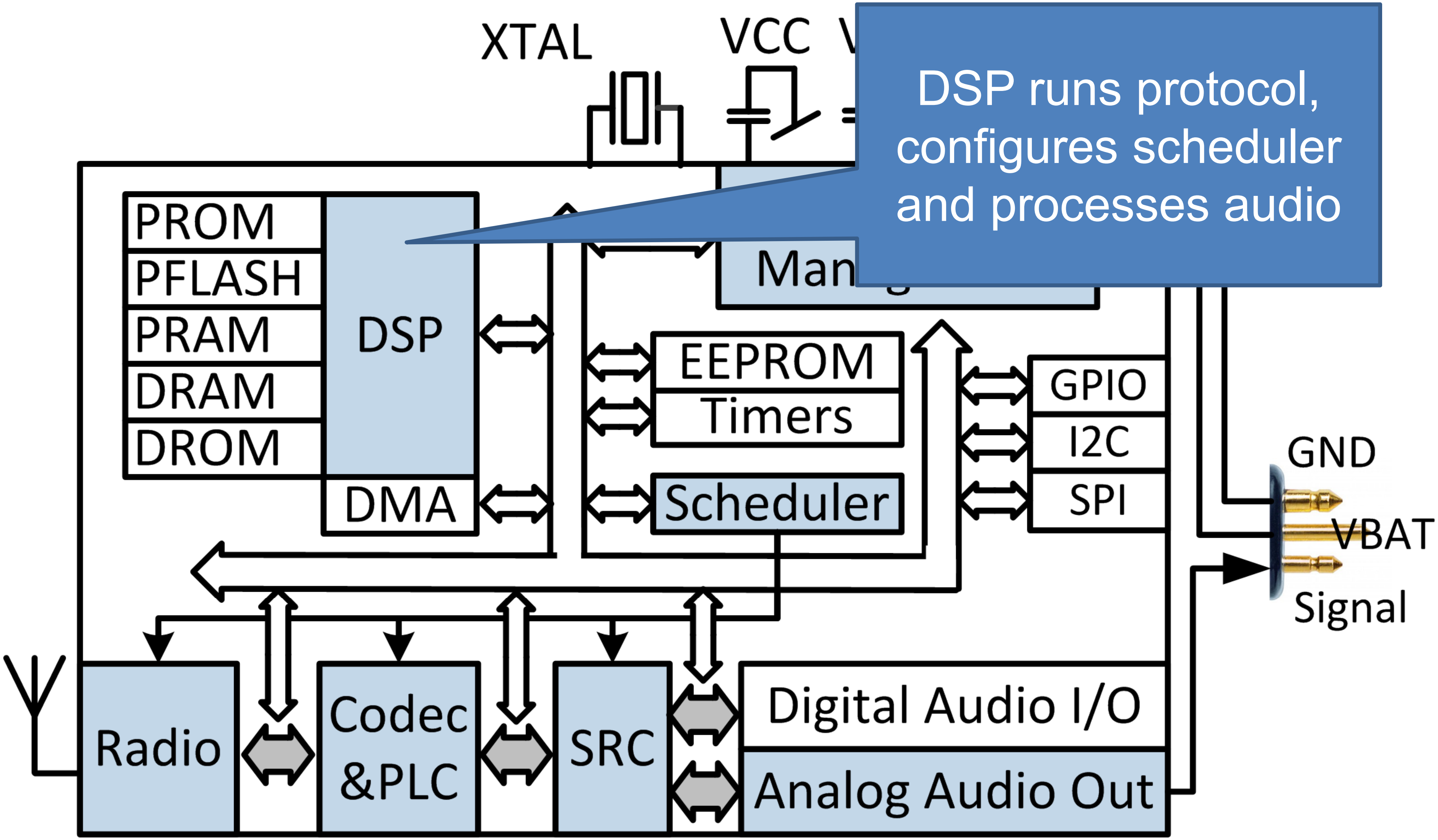
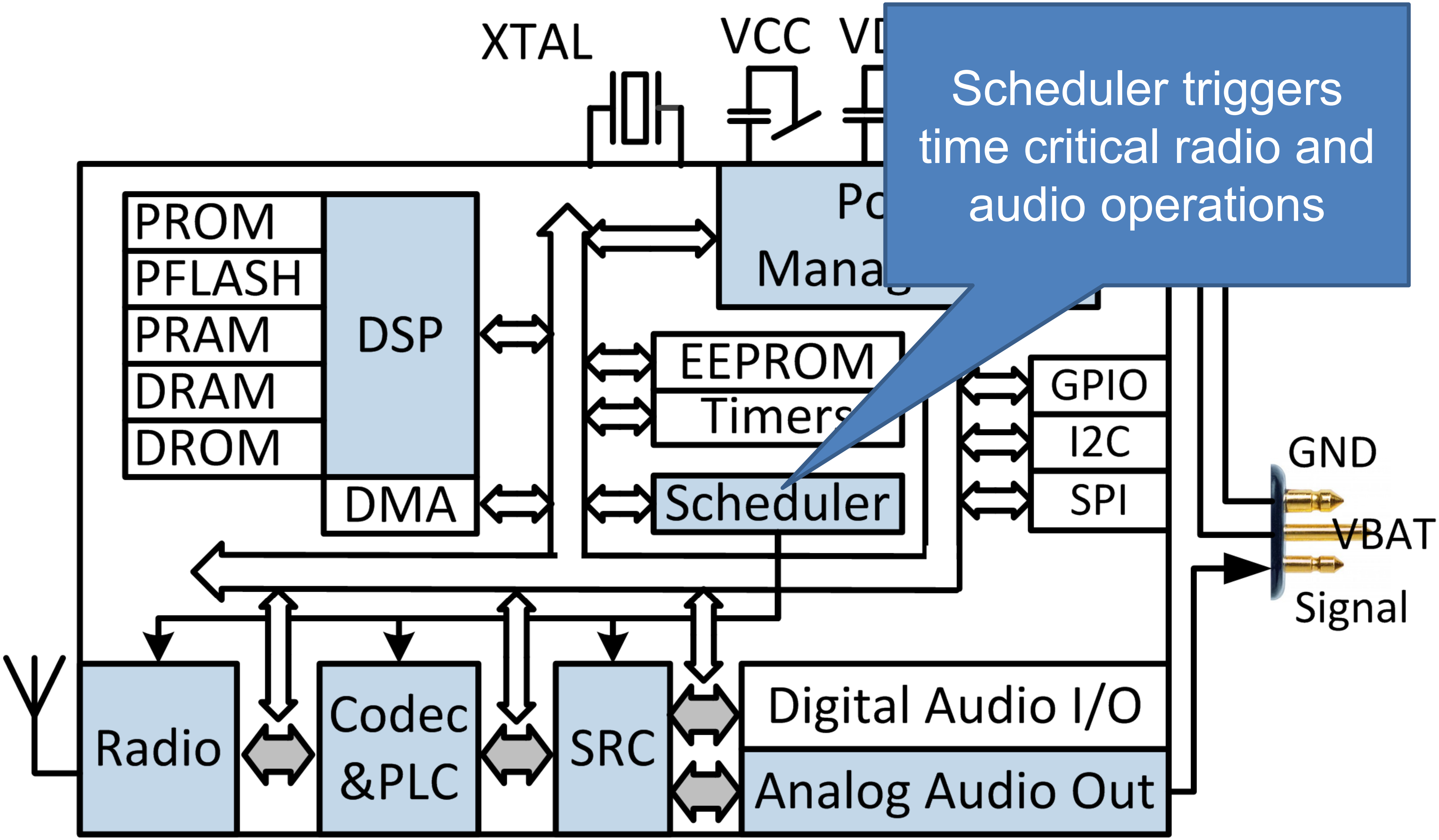


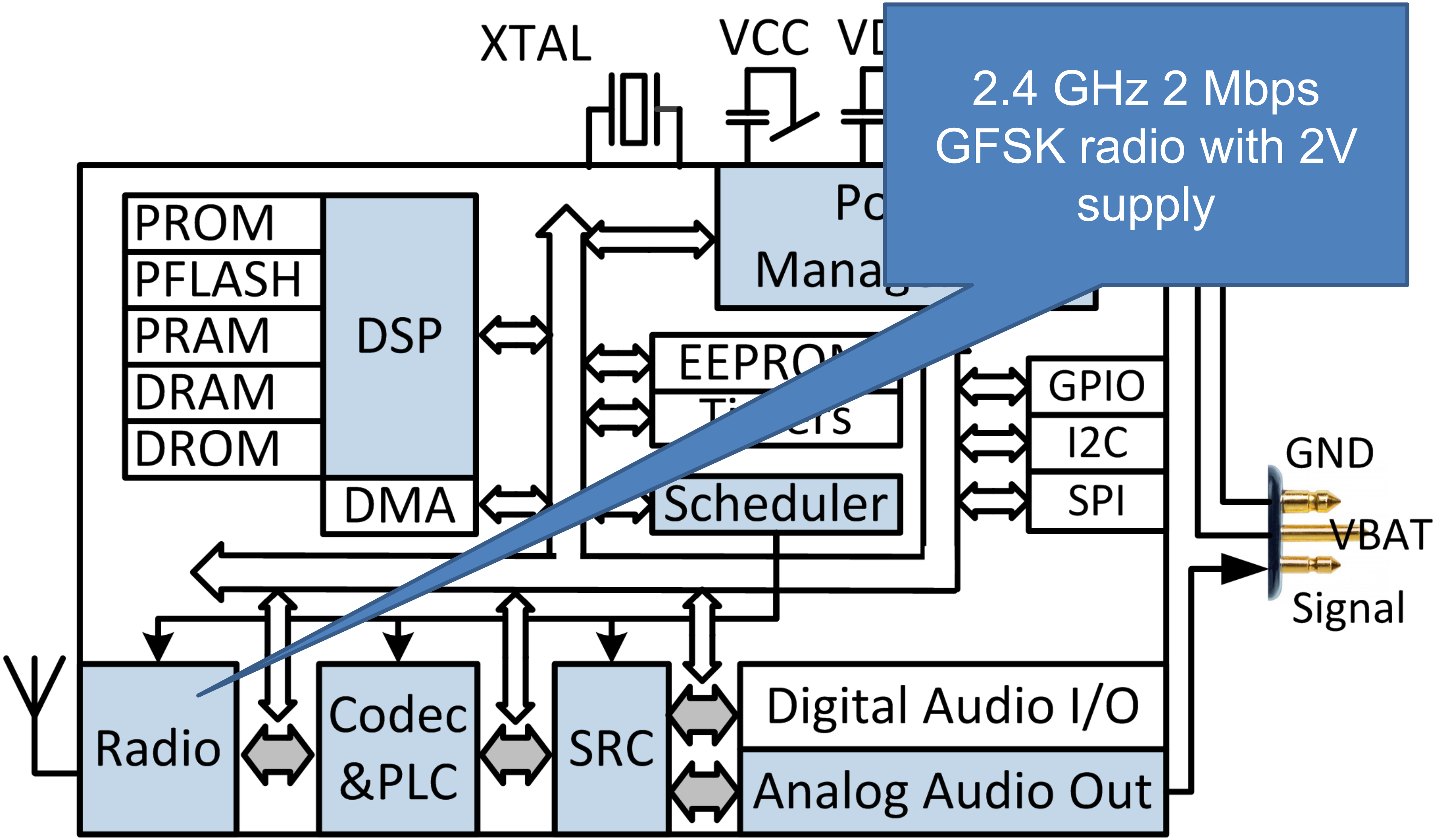
DSP runs protocol, configures scheduler and processes audio

Wireless Audio SoC Block Diagram



Scheduler triggers time critical radio and audio operations

Wireless Audio SoC Block Diagram



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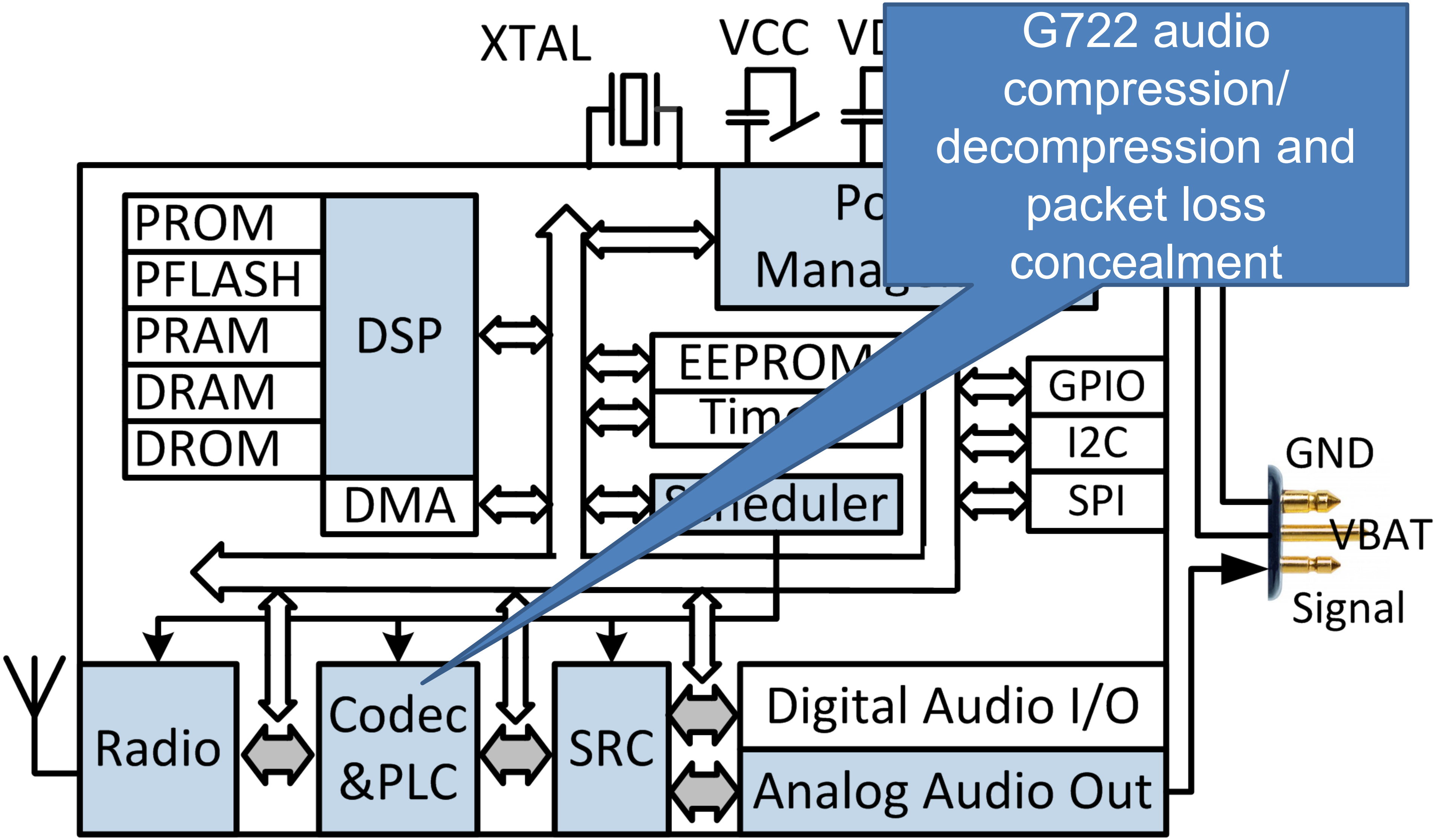

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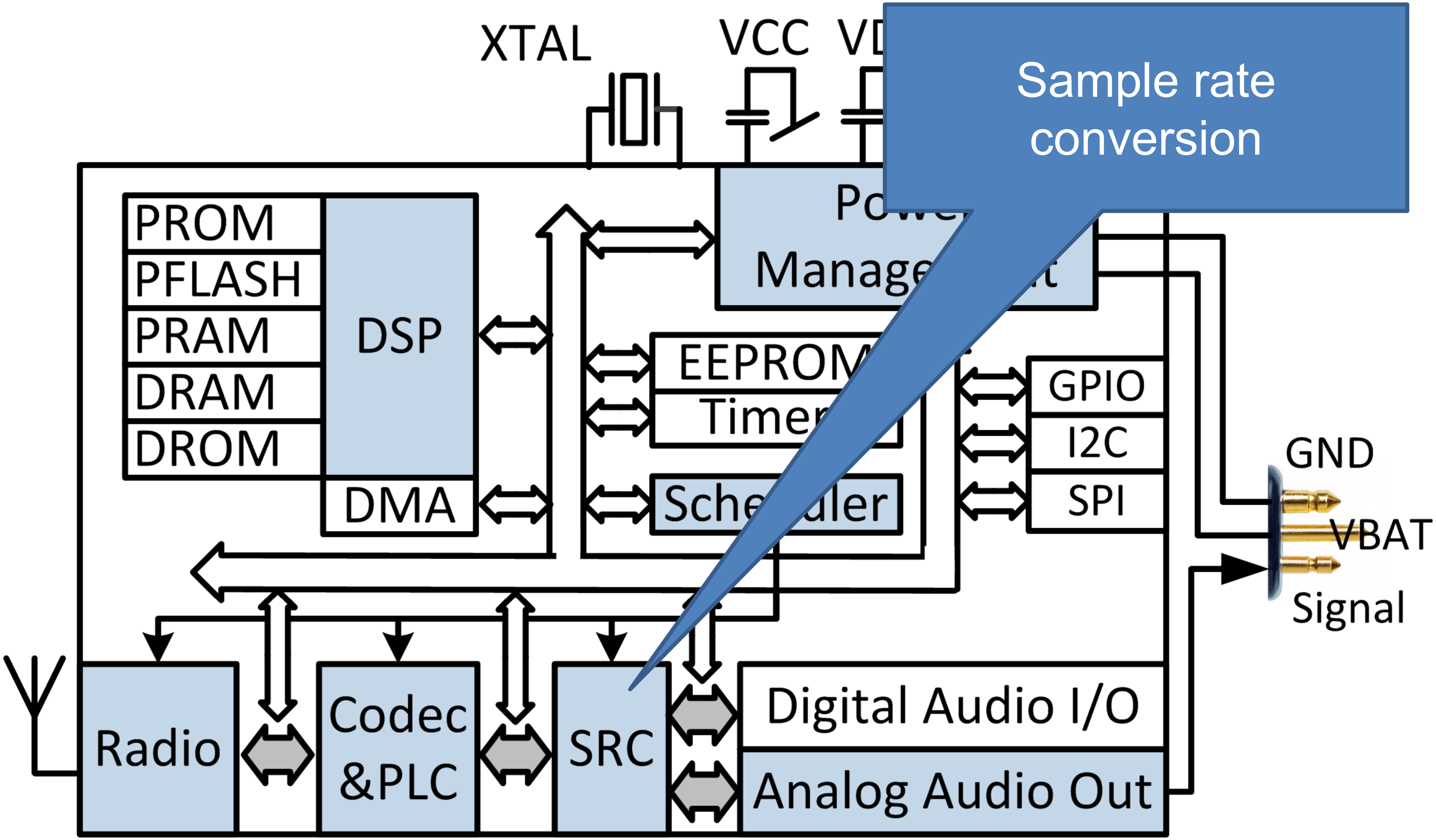

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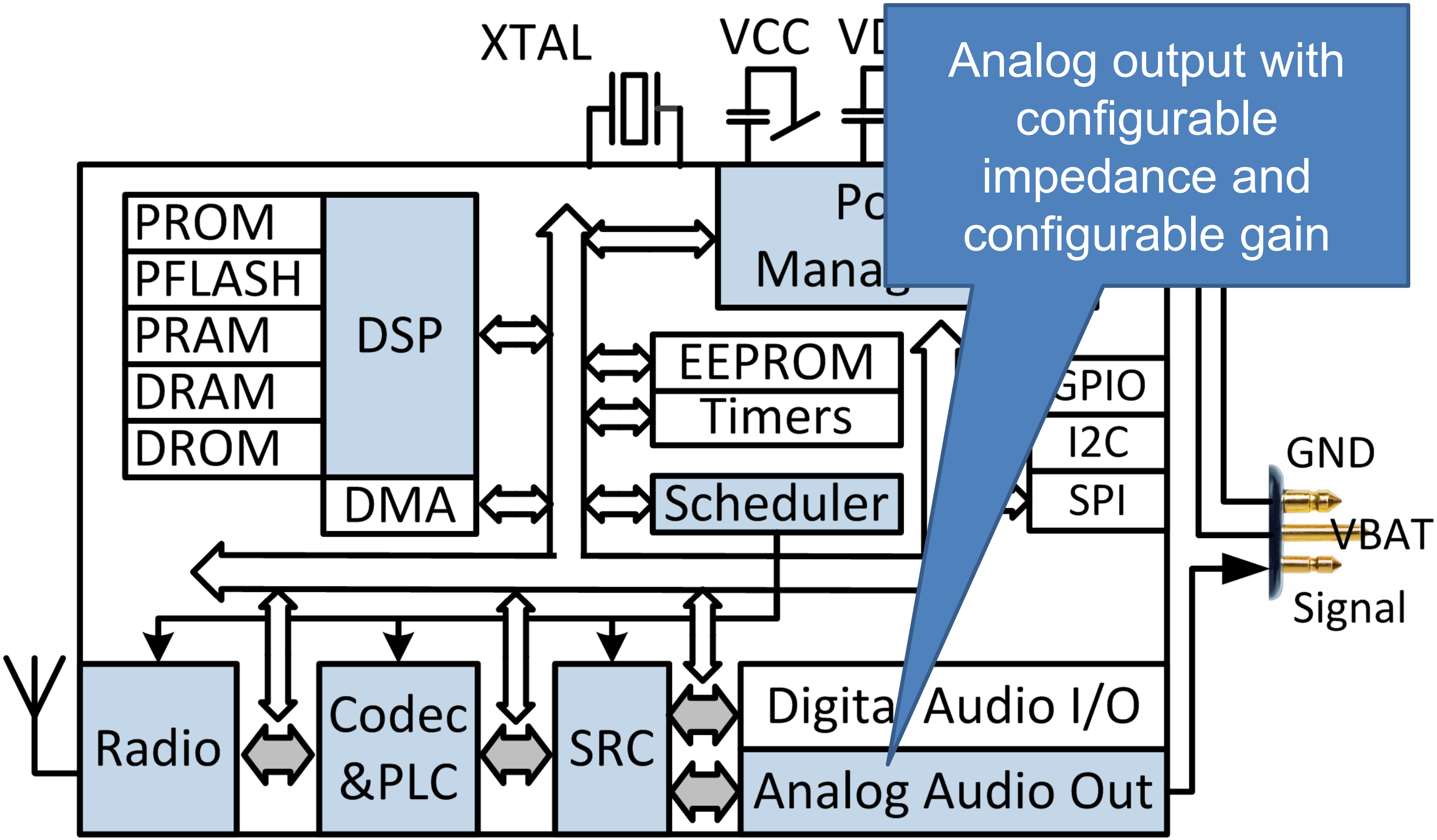
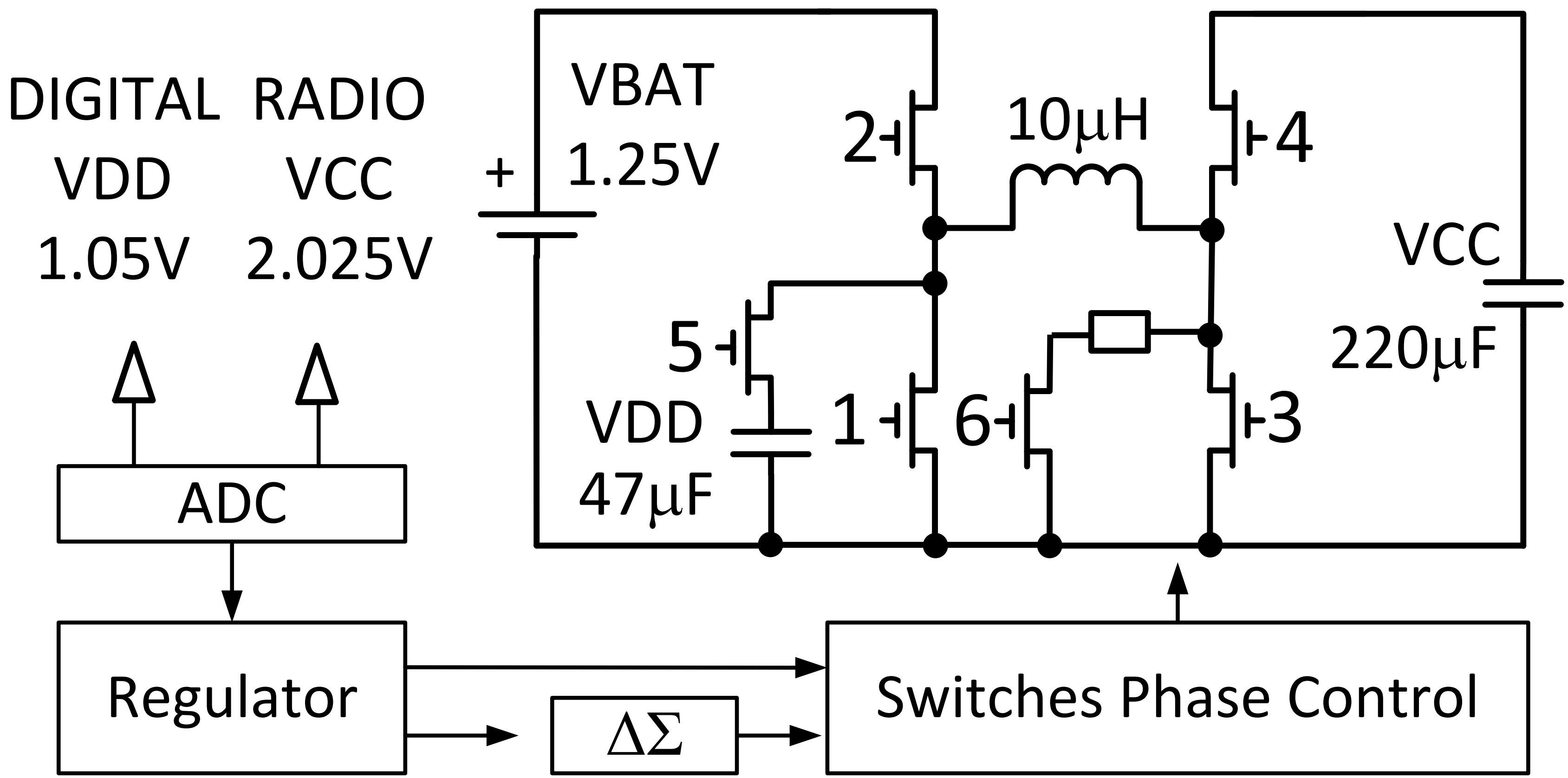
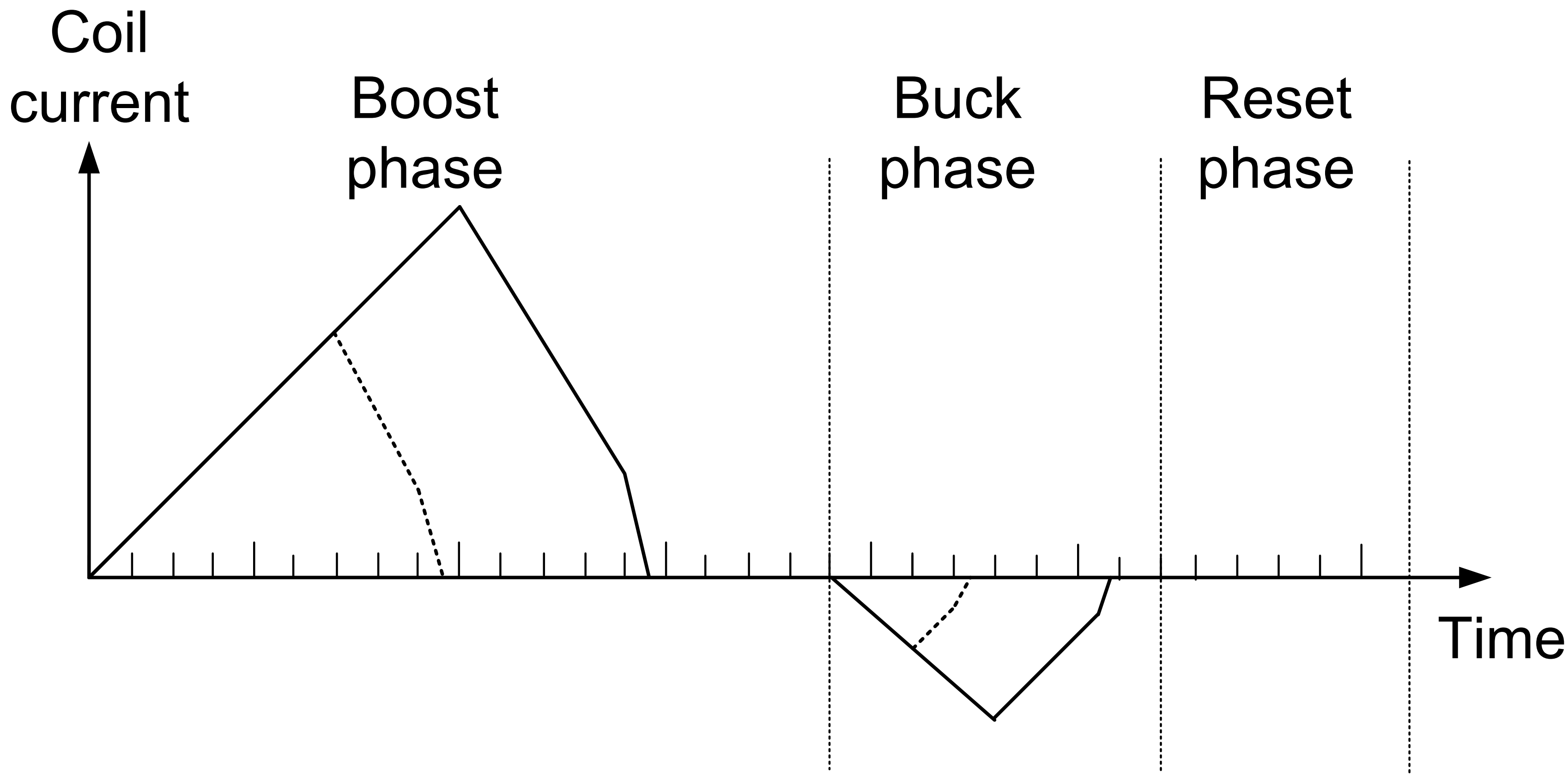


Power Management Schematics

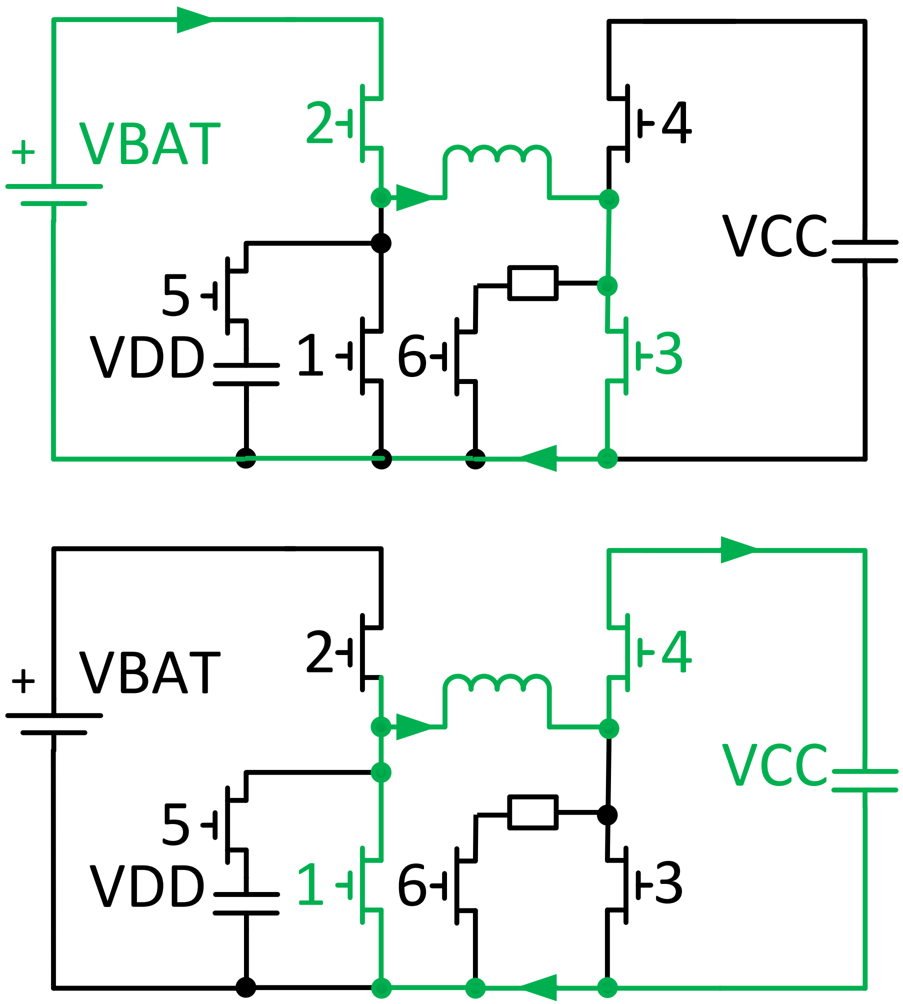


See US20130129126A1, Francois Callias *et al.*

Converter Phases

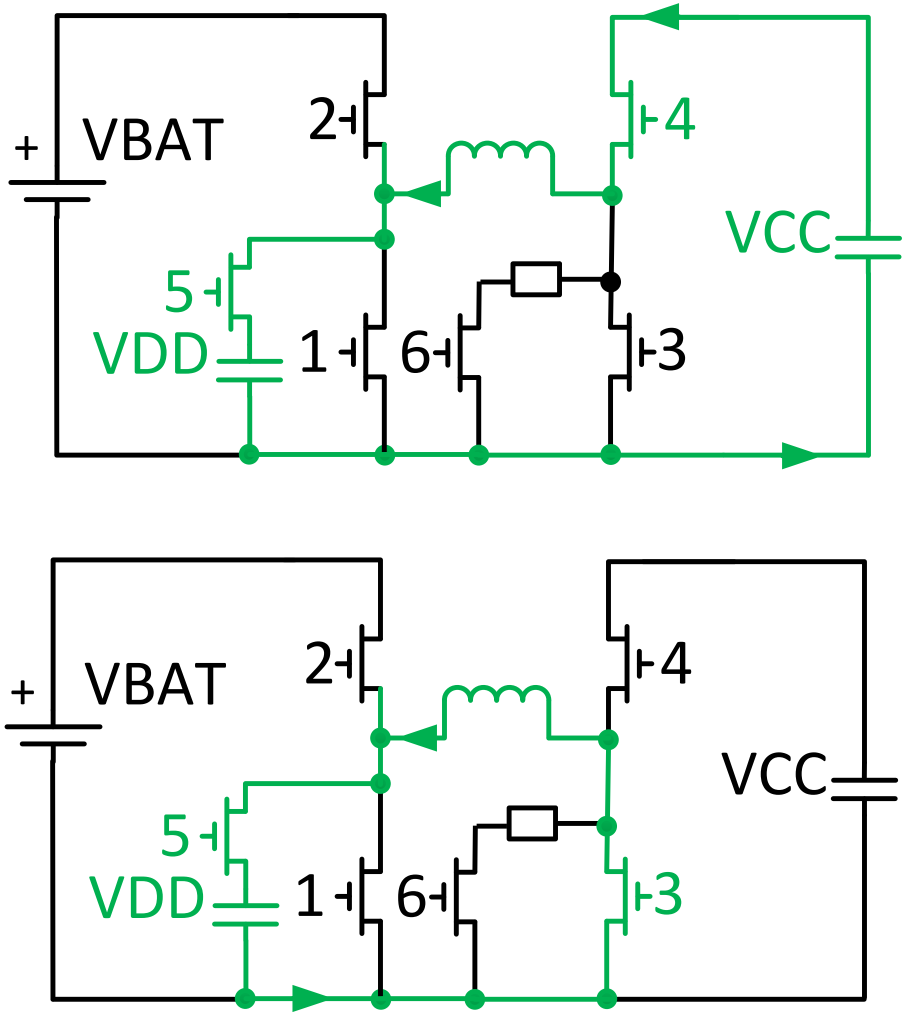


Boost Phase



- Current launched into the coil from VBAT
- Current filled into VCC cap from GND
- 75% VCC efficiency

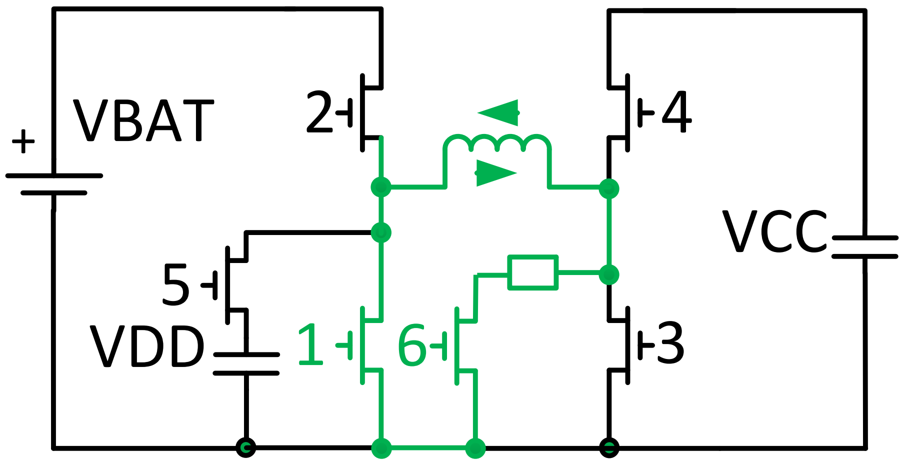
Buck Phase



- Current launched into the coil from VCC (to isolate from VBAT)

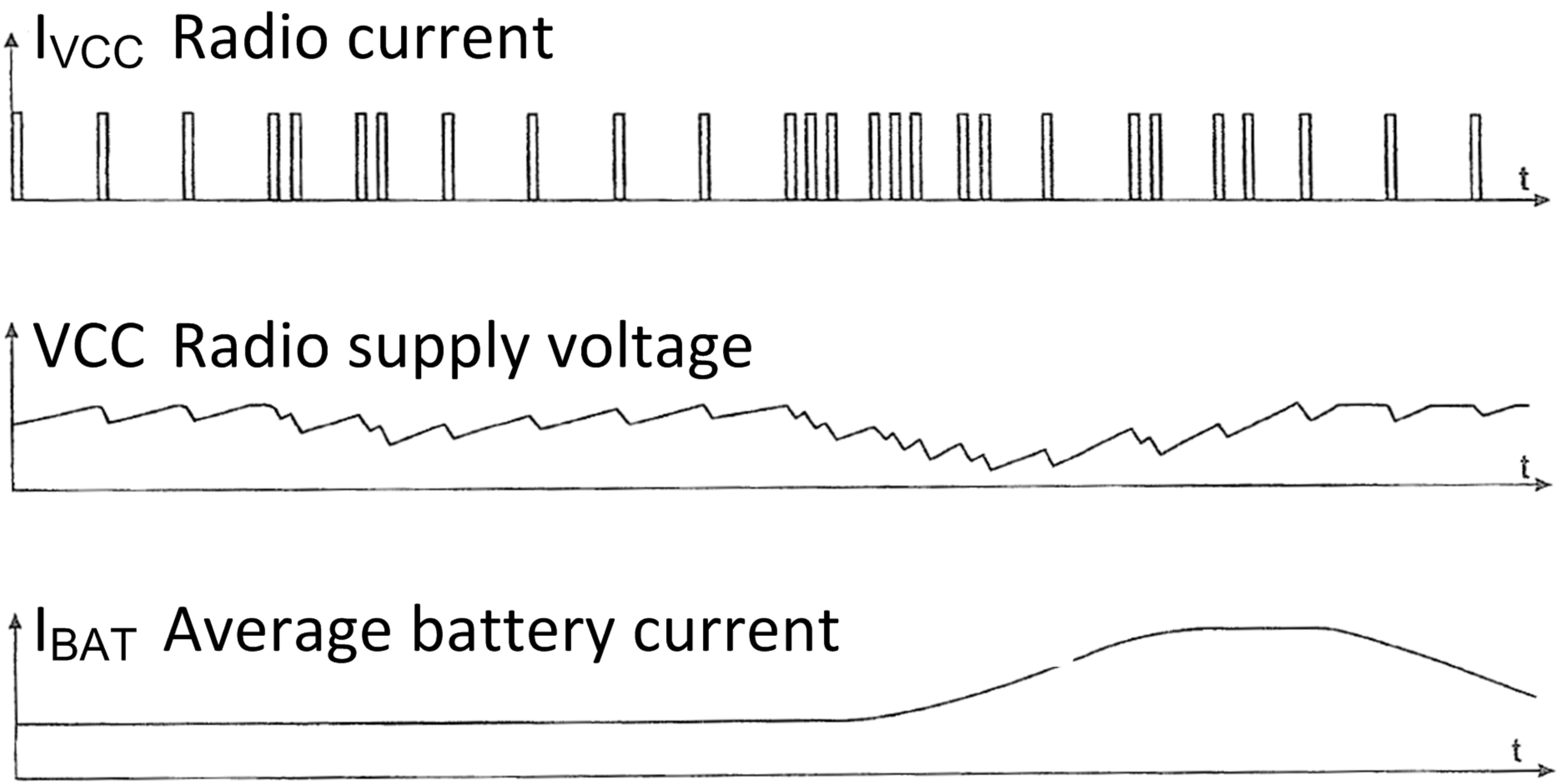
- 86% VDD eff. from VCC
- 65% VDD eff. from VBAT

Reset Phase

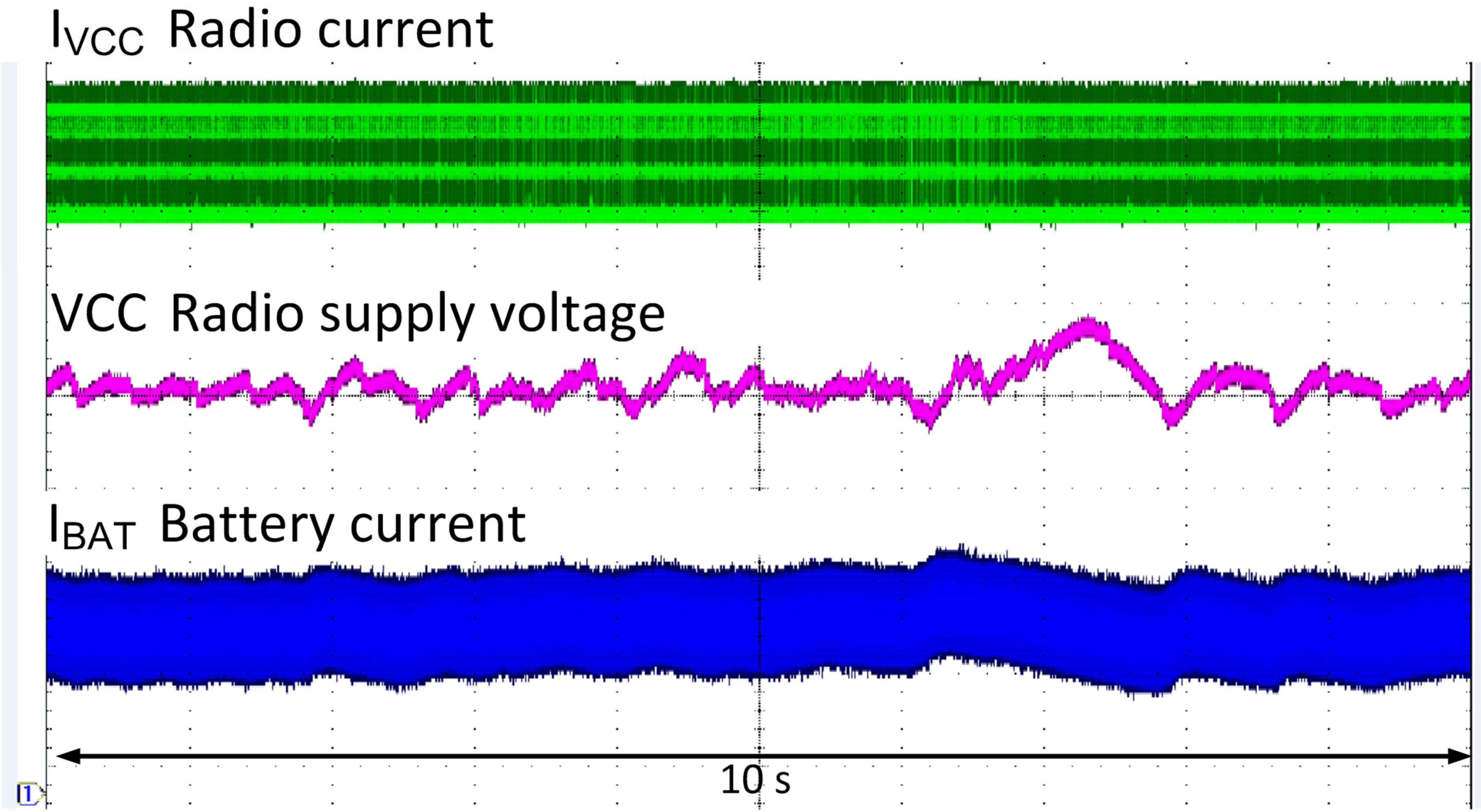


- Residual oscillating current damped into a resistor.

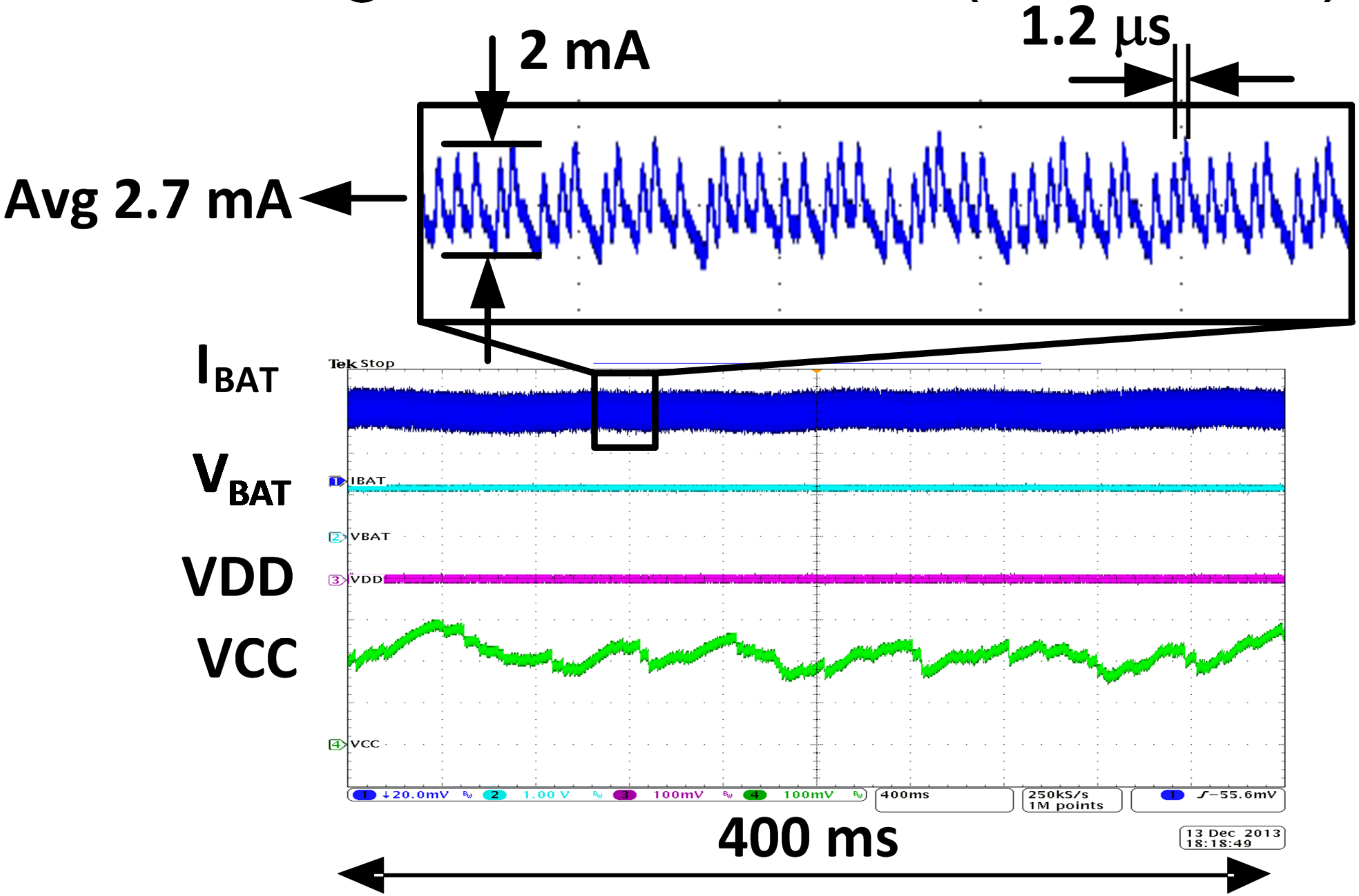
Slow average battery current consumption variation - Principle



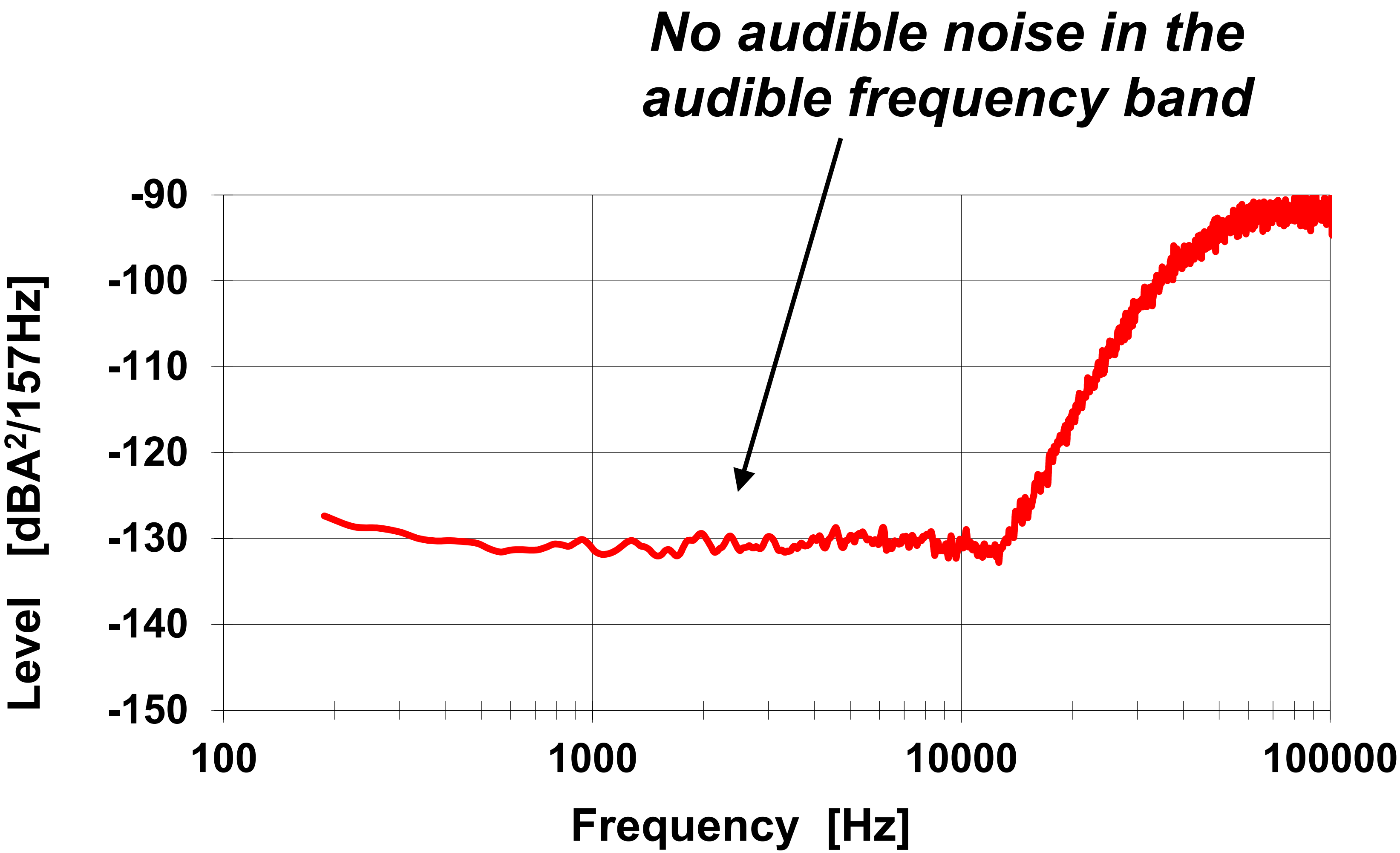
Slow average battery current consumption variation - Measurement



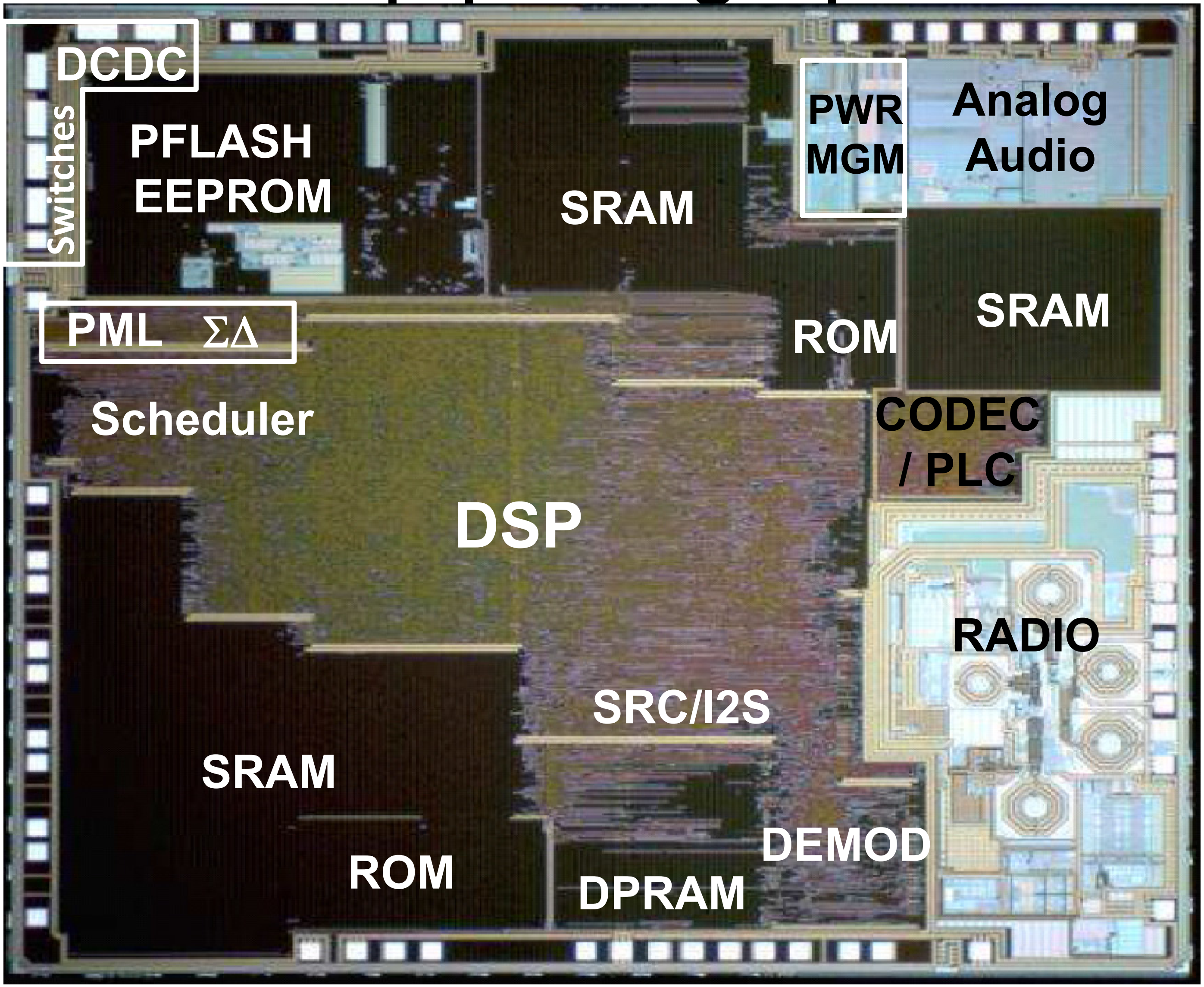
Resulting VBAT Current (Mono Rx)



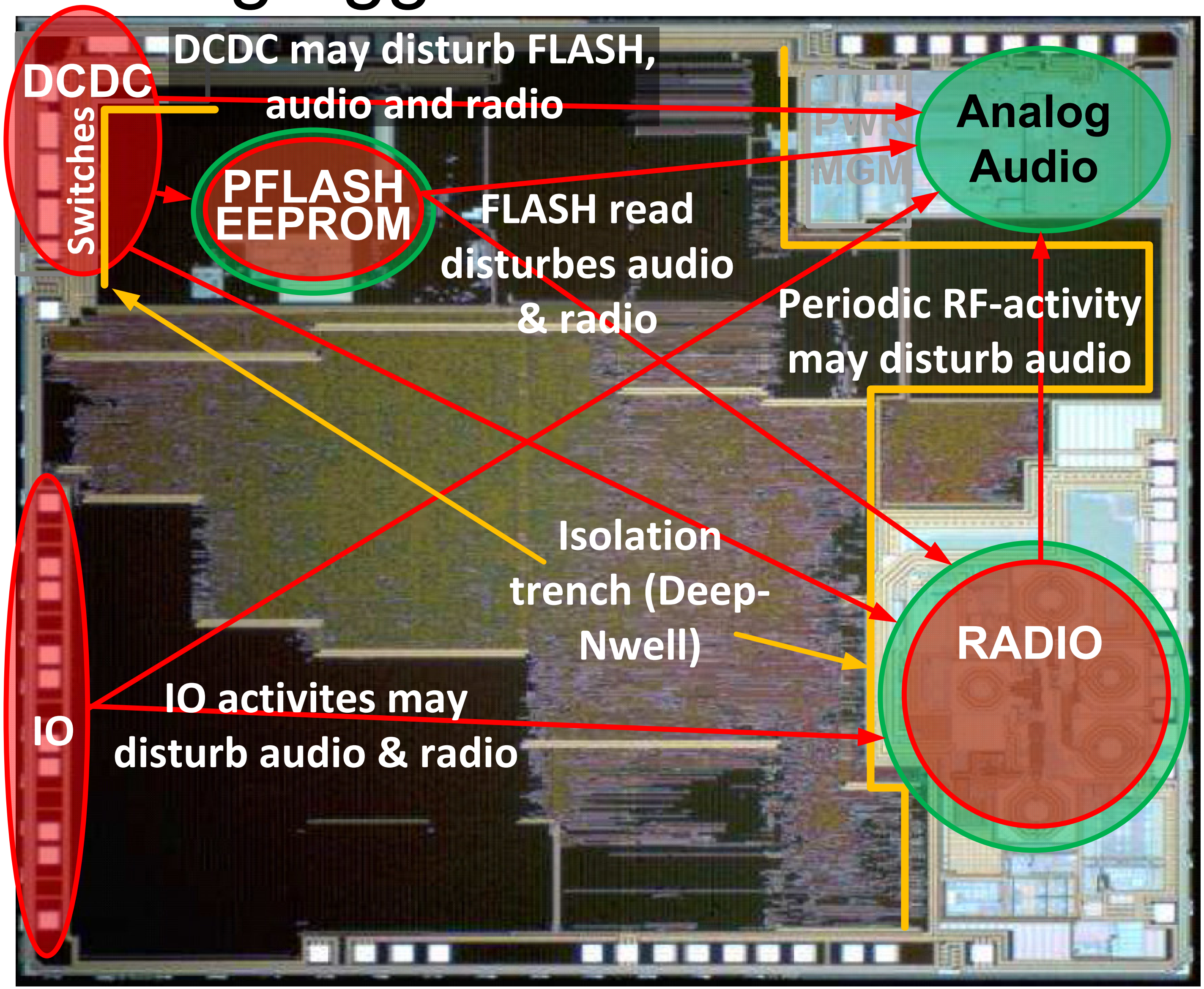
Resulting VBAT Current Spectrum



Chip photograph



Maximizing aggressor/victim distance



Summary

Wireless audio digital communication SoC

- Single chip solution (including NVM)
- Radio @ 2.4 GHz, 2 Mbps, GFSK
- Supply from 1V-1.4V
- Single inductor dual output DC/DC converter avoiding audible battery current ripple
- 2.7mA@1.25V avg battery current for 7kHz BW audio RX

➔ Enables miniaturized wireless receivers for hearing aid applications

➔ Other applications: Mono or stereo audio transmitters, Full duplex audio, 14 kHz audio BW

Acknowledgements

We would like to acknowledge the contributions of all team members:

- EM Microelectronic - Marin, Switzerland and USA
- ASICentrum, Prague, Czech Republic
- Phonak, Murten & Stäfa, Switzerland
- External contractors

Questions ?

A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18μm HVCMOS

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[1]*Massachusetts Institute of Technology*
[2]*Harvard Medical School*
[3]*Massachusetts Eye and Ear Infirmary*

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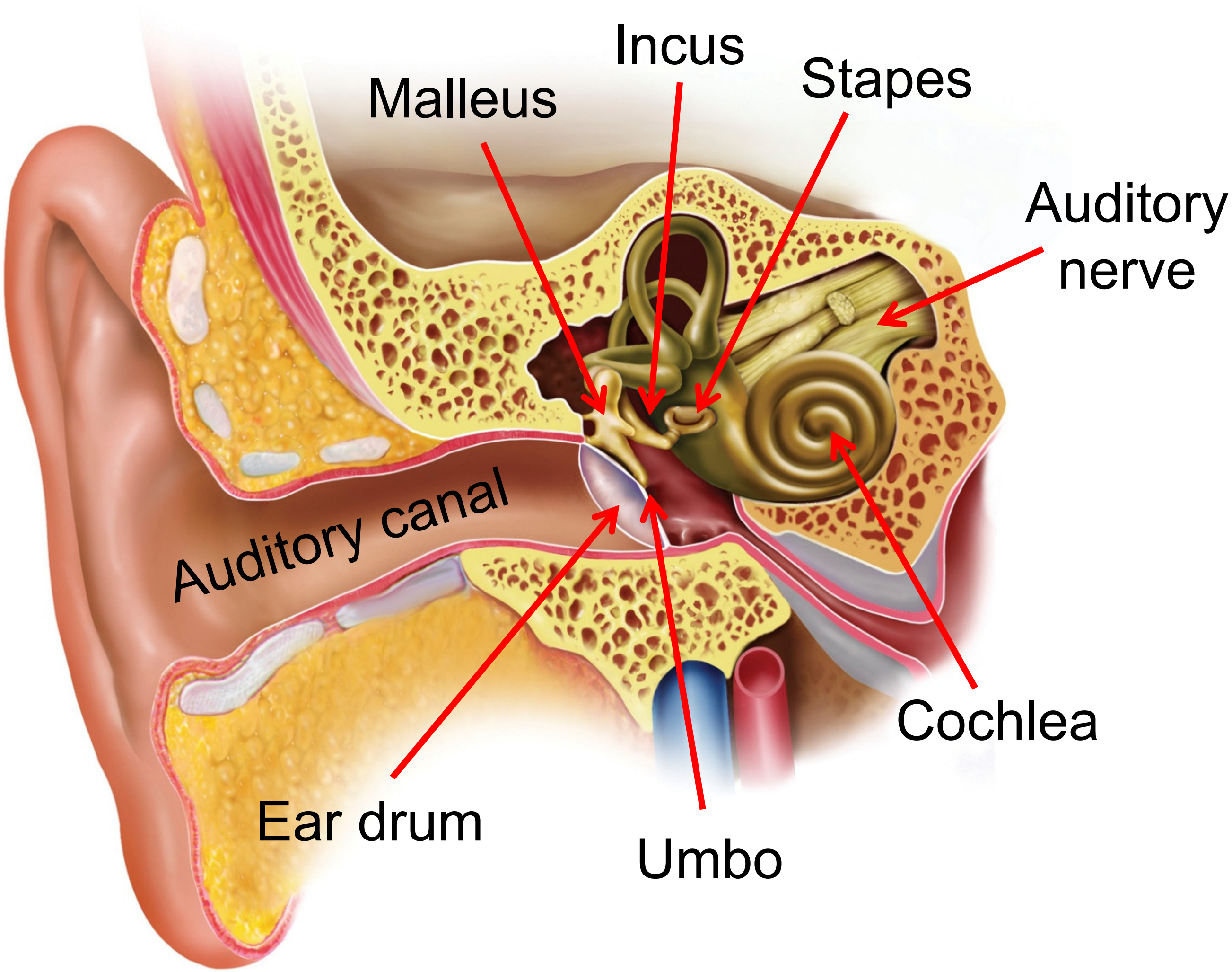
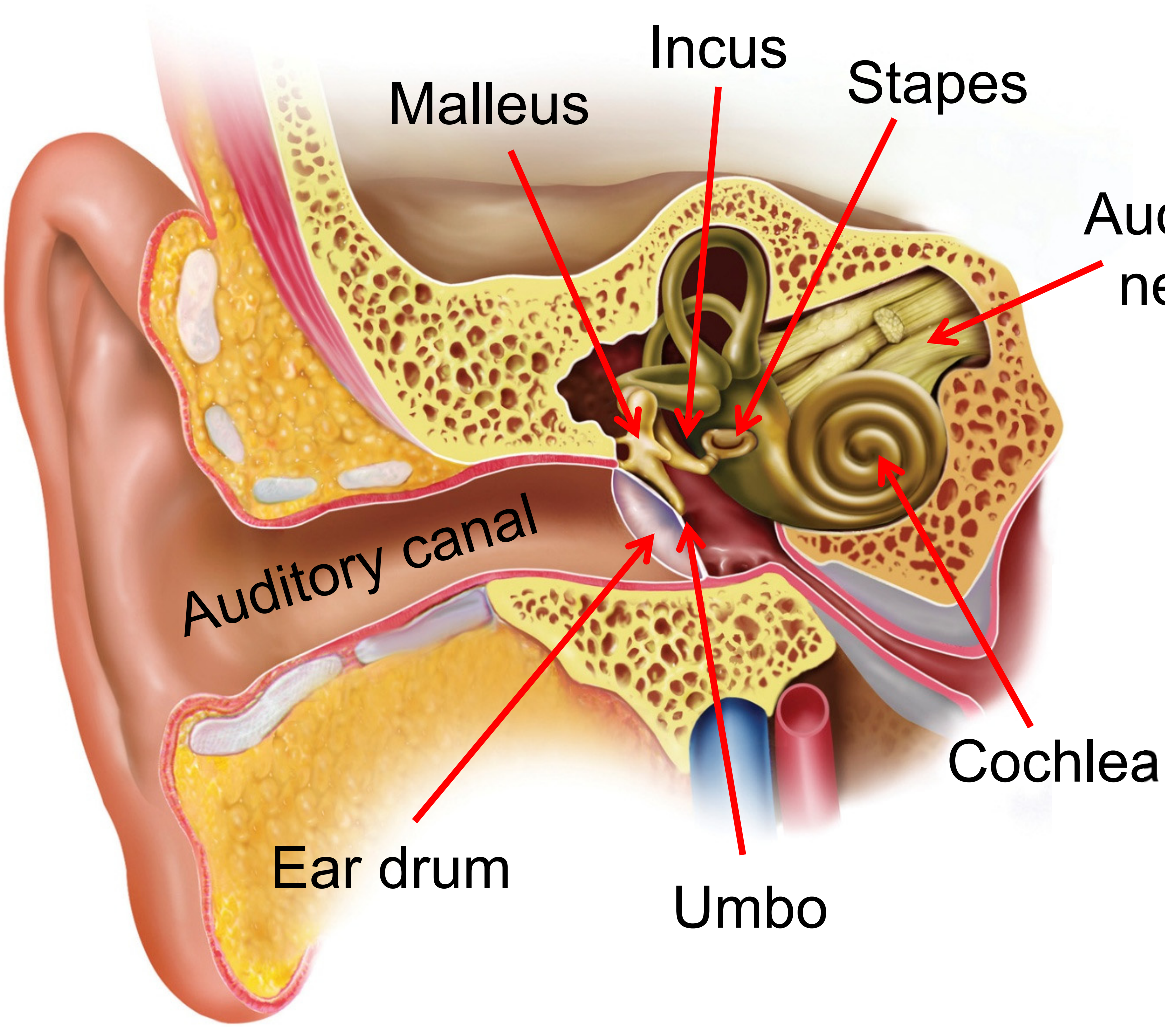
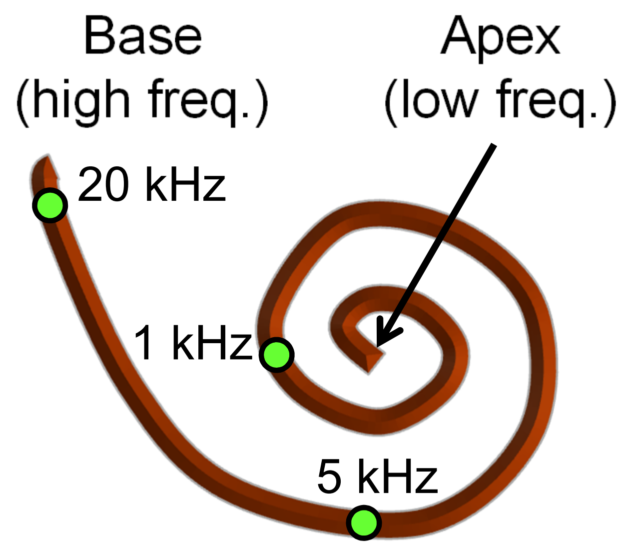
Review: Anatomy of the Ear



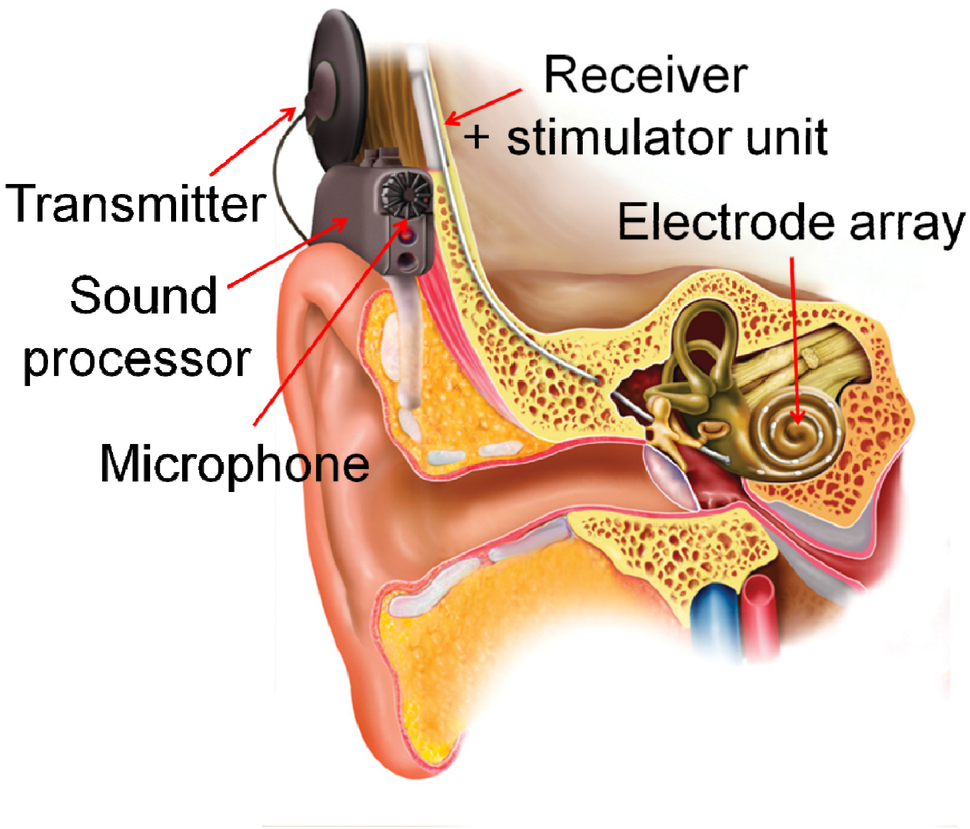
Review: Anatomy of the Ear



Cochlea is frequency selective



Limitations of Conventional Cochlear Implants



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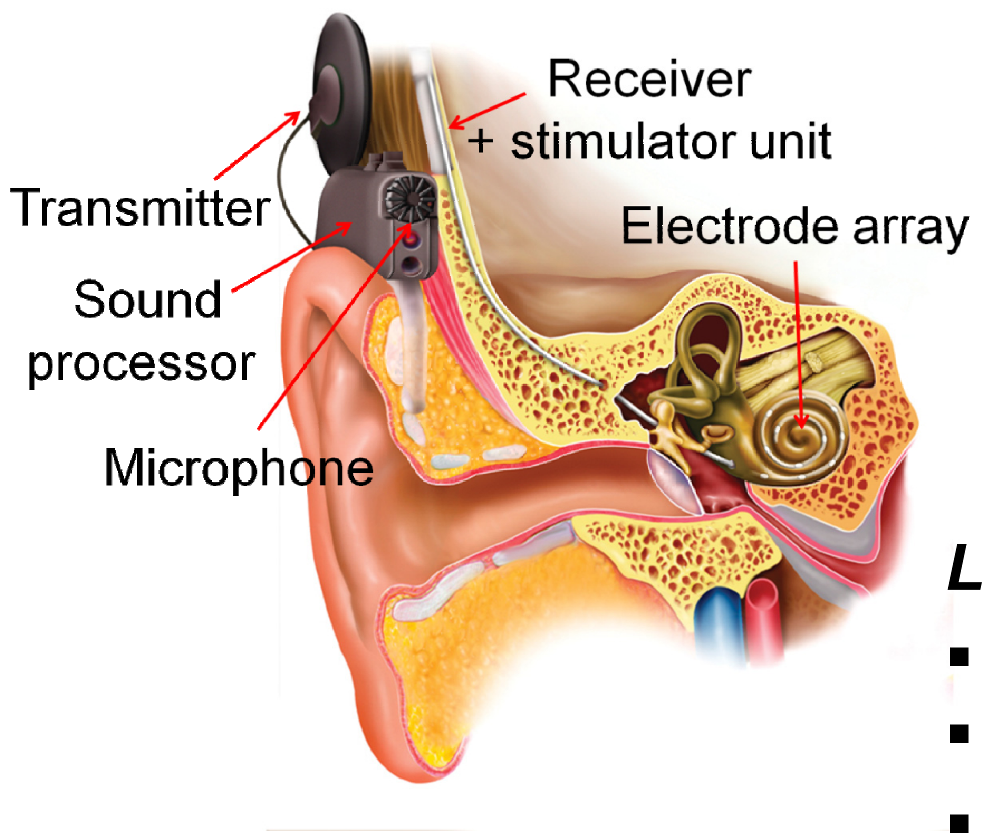


Limitations

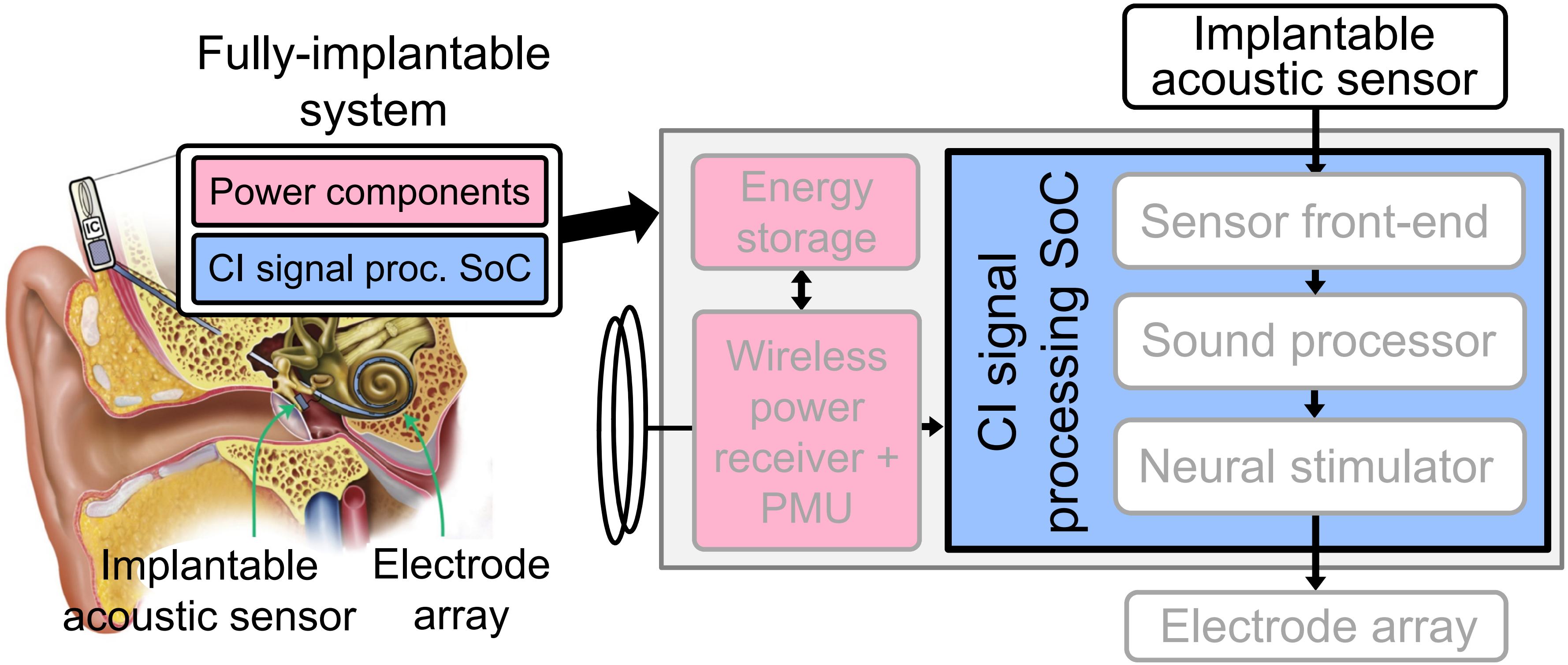
- Cumbersome
- Usage in shower/water sports
- Aesthetics and social stigma

A fully-implantable (i.e., internalized & invisible) solution is highly desirable

Outline

- Challenges and system overview
- SoC architecture
  - Implantable piezoelectric acoustic sensor
  - Reconfigurable sound processor
  - Energy-efficient arbitrary waveform neural stimulator
- Measurement results
  - Demonstration with human cadaveric specimen
- Conclusion

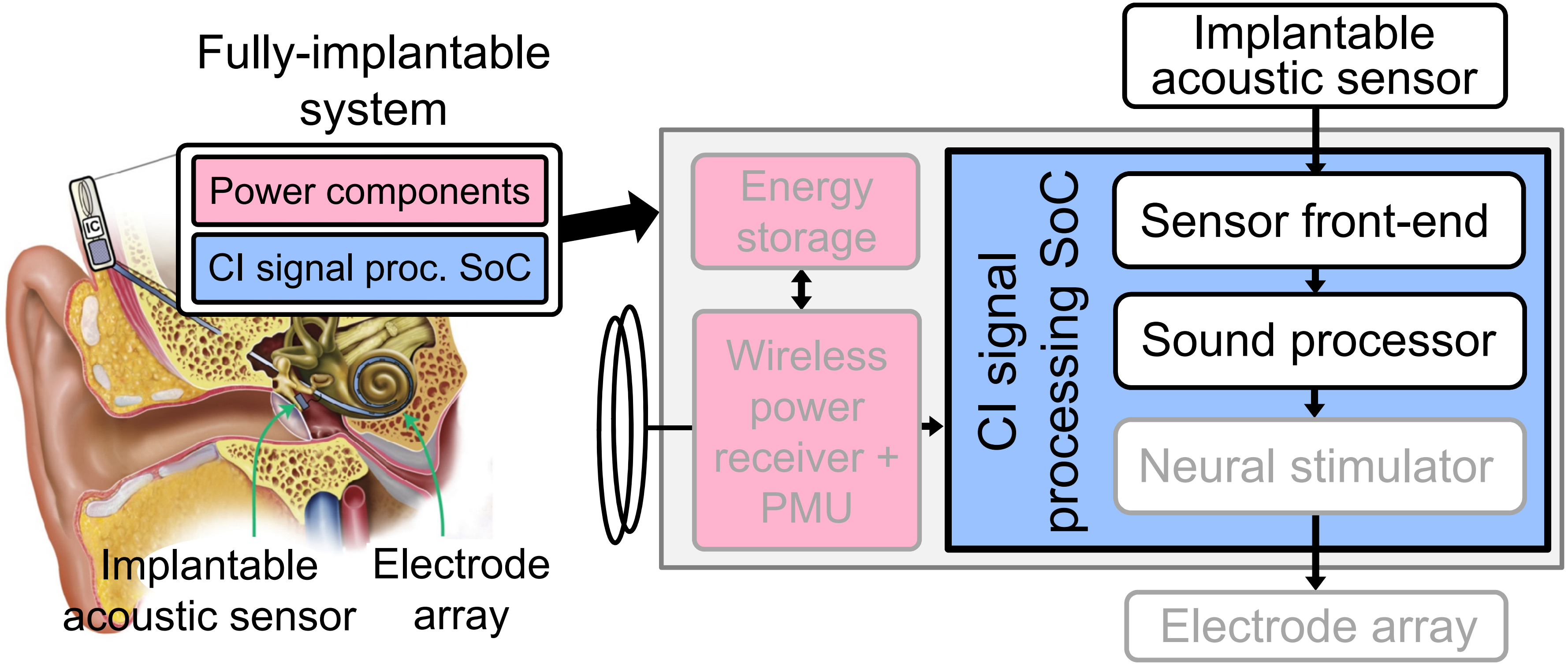
Challenges and Overview of a Fully-Implantable CI



Challenges of a fully-implantable solution:

1. Implantable acoustic sensor

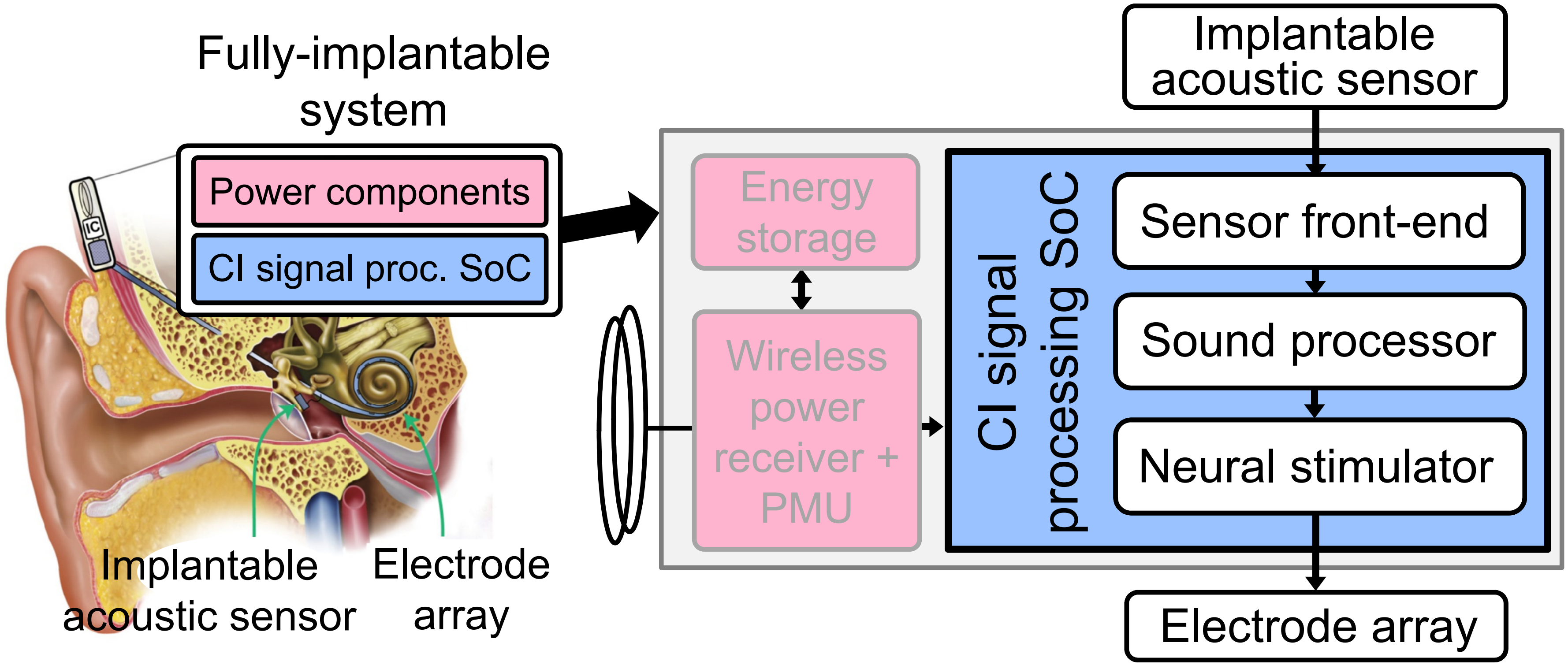
Challenges and Overview of a Fully-Implantable CI



Challenges of a fully-implantable solution:

1. Implantable acoustic sensor
2. ULP sensor front-end and sound processor

Challenges and Overview of a Fully-Implantable CI



Challenges of a fully-implantable solution:

1. Implantable acoustic sensor
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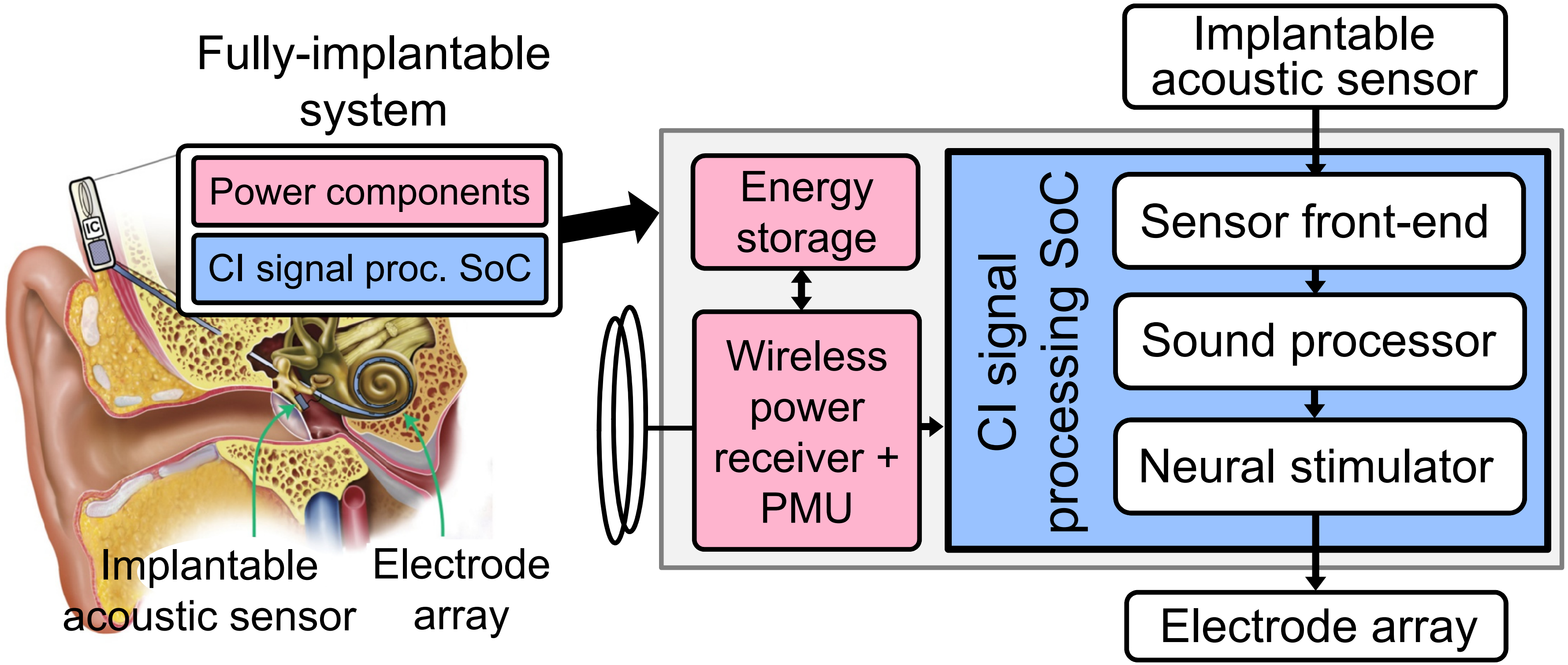
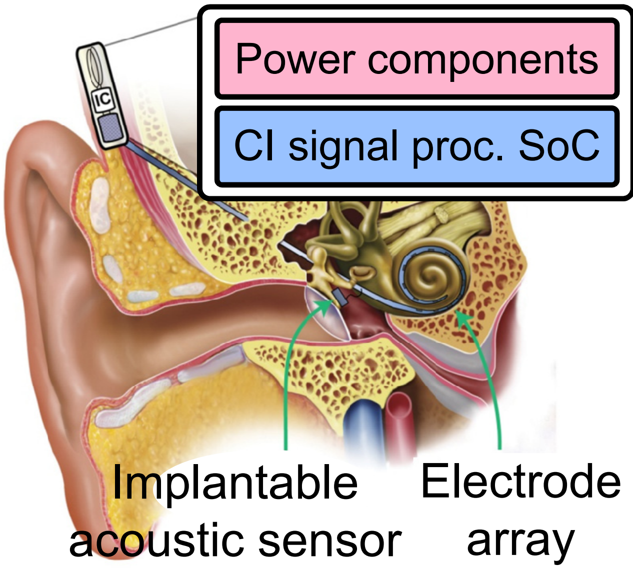
Challenges and Overview of a Fully-Implantable CI

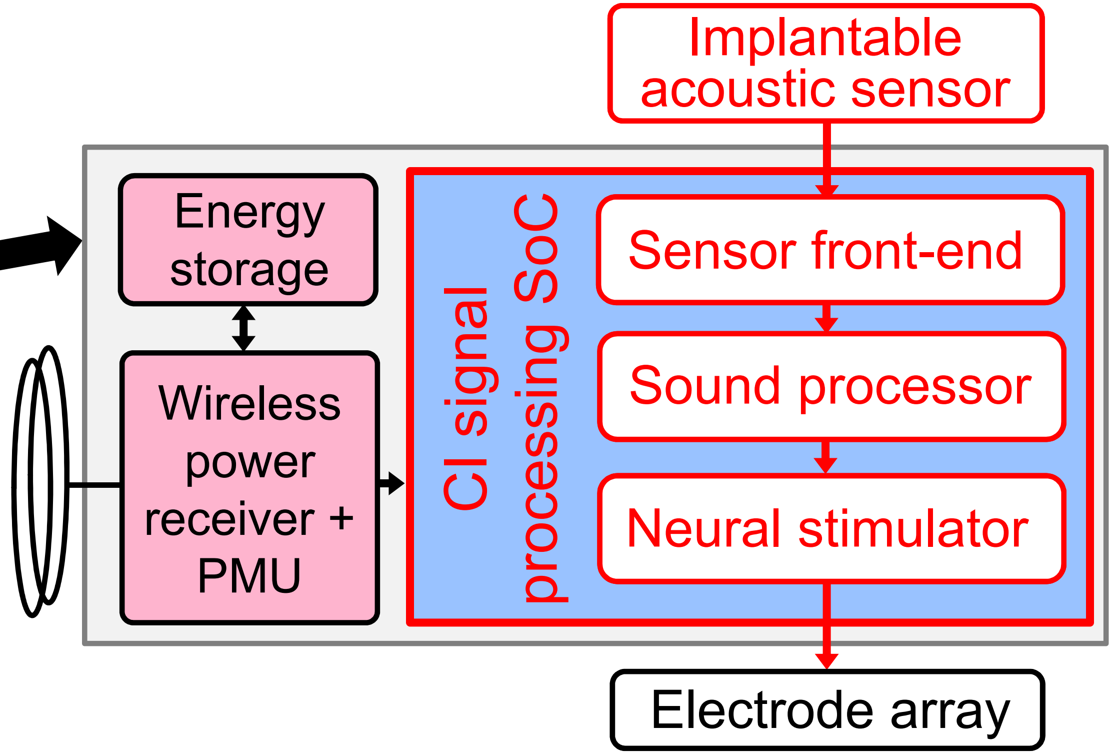


Challenges of a fully-implantable solution:

1. Implantable acoustic sensor
2. ULP sensor front-end and sound processor
3. Energy-efficient neural stimulation
4. Wireless power delivery and management

Challenges and Overview of a Fully-Implantable CI



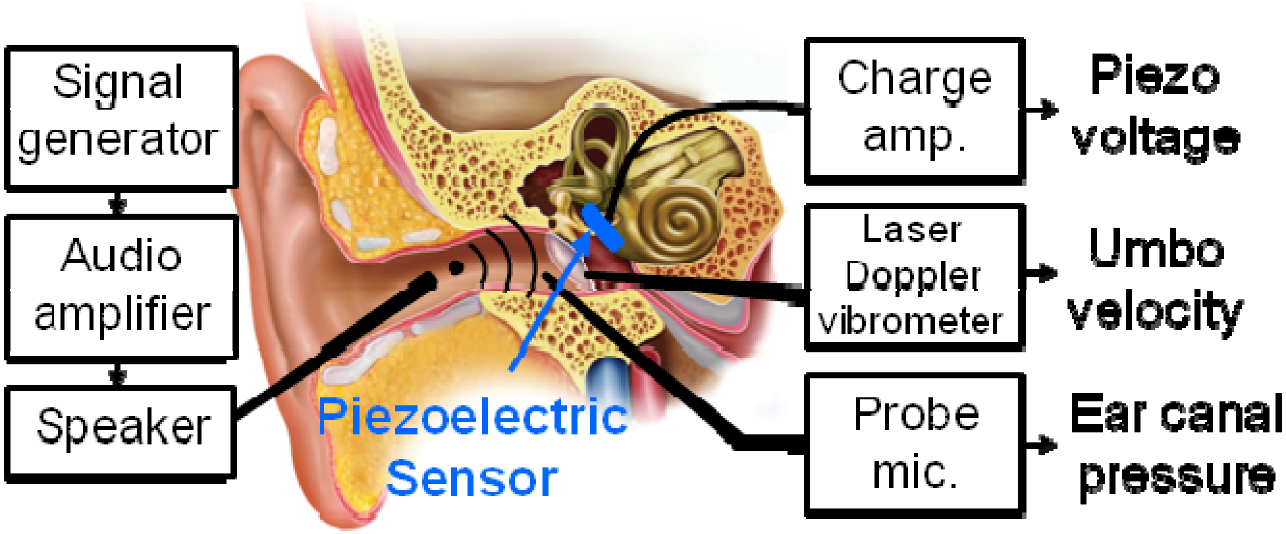


Challenges of a fully-implantable solution:

1. Implantable acoustic sensor
2. ULP sensor front-end and sound processor
3. Energy-efficient neural stimulation
4. Wireless power delivery and management

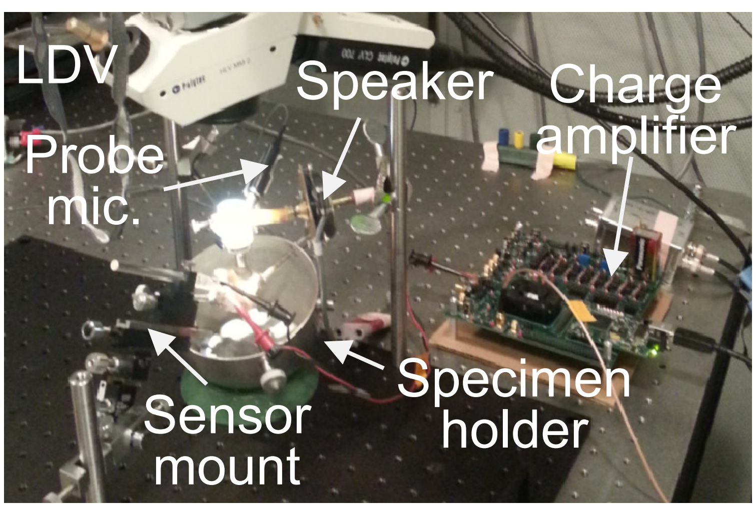
SoC in this work

Piezoelectric Acoustic Sensor

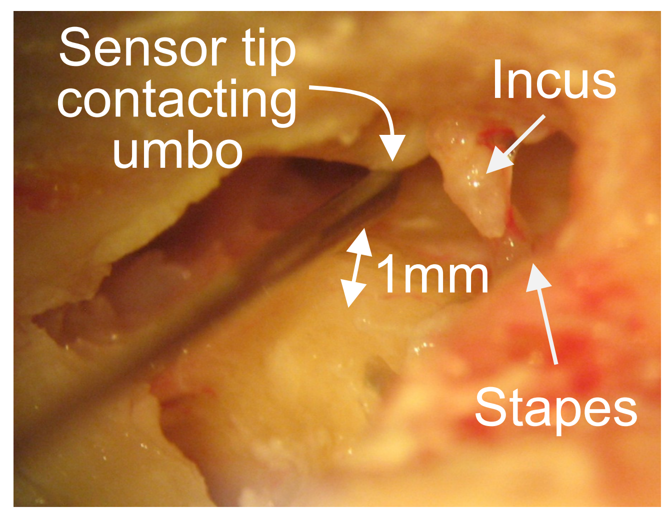


Acoustical
↓
Mechanical
↓
Electrical

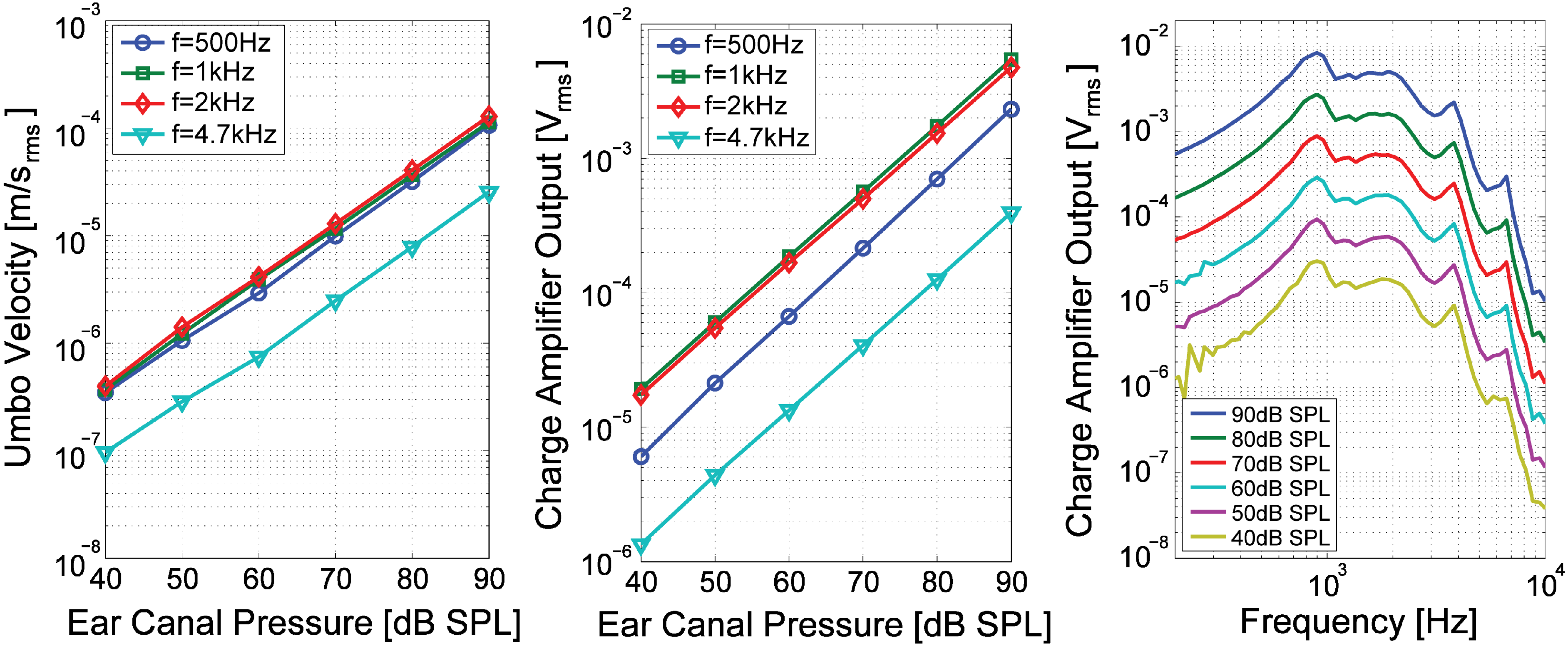
Photograph of test setup



Close-up of middle ear

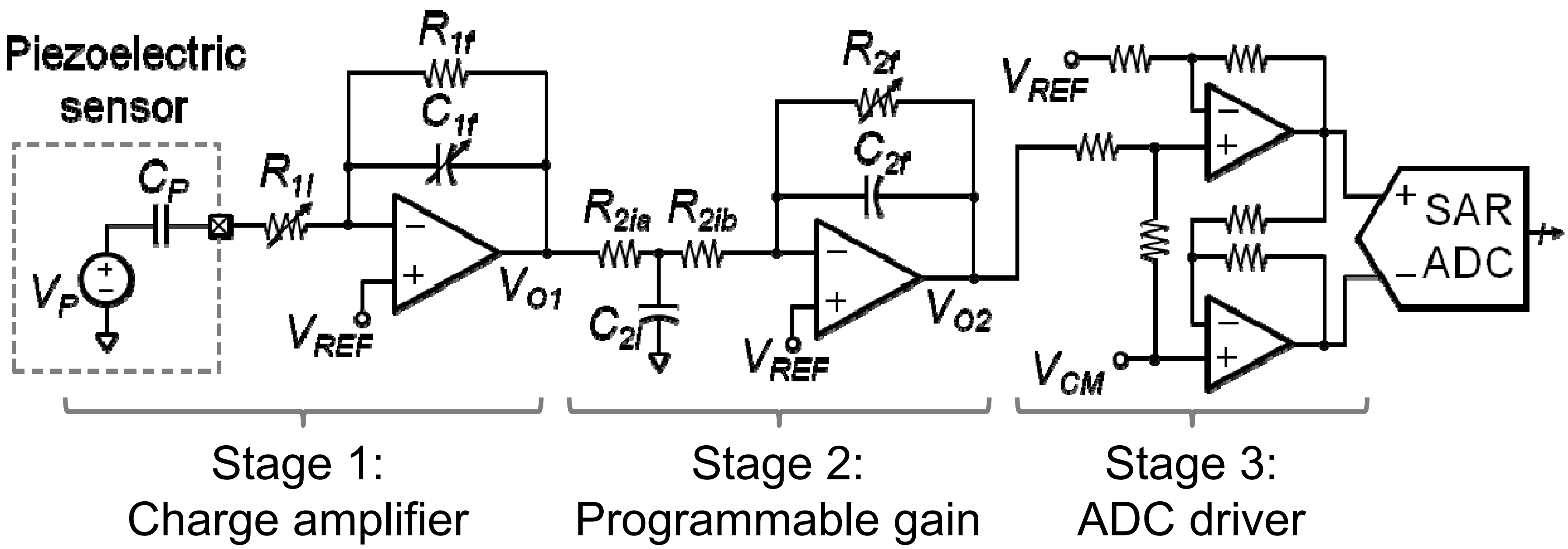


Sensor Characterization

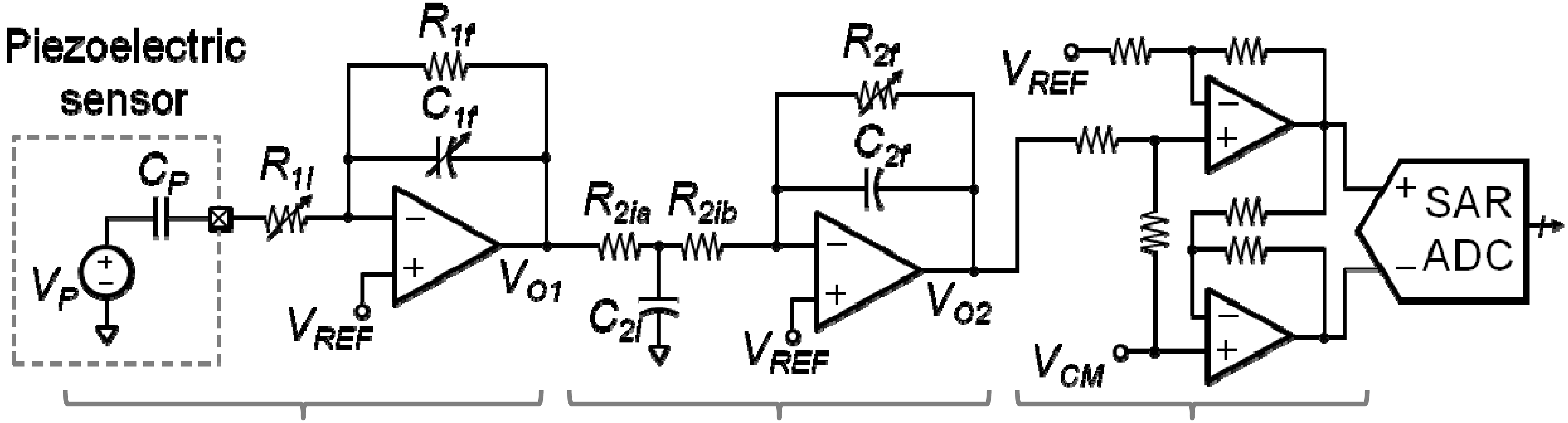


- Middle ear mechanics and sensor show excellent linearity
- Sensitivity down to 40 dB SPL @ 300Hz

Integrated Sensor Front-End



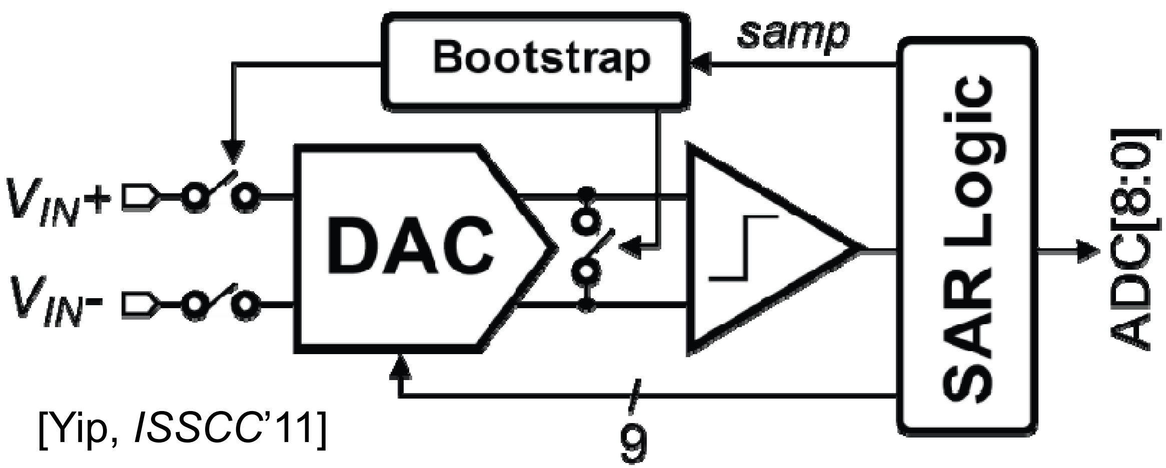
Integrated Sensor Front-End



Stage 1:
Charge amplifier

Stage 2:
Programmable gain

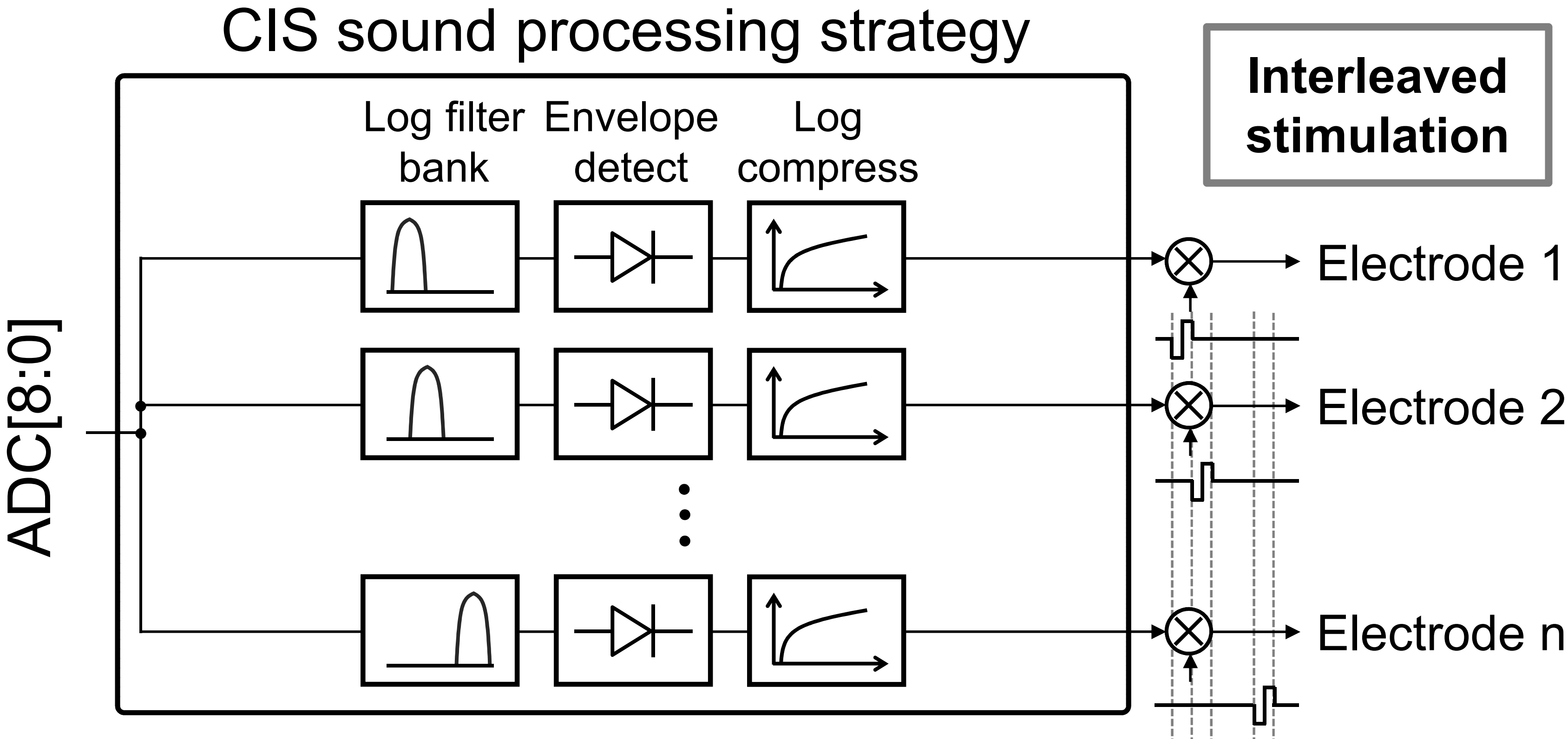
Stage 3:
ADC driver



V_{DD}	0.6V
Resolution	9 bits
Sampling rate	16 kS/s

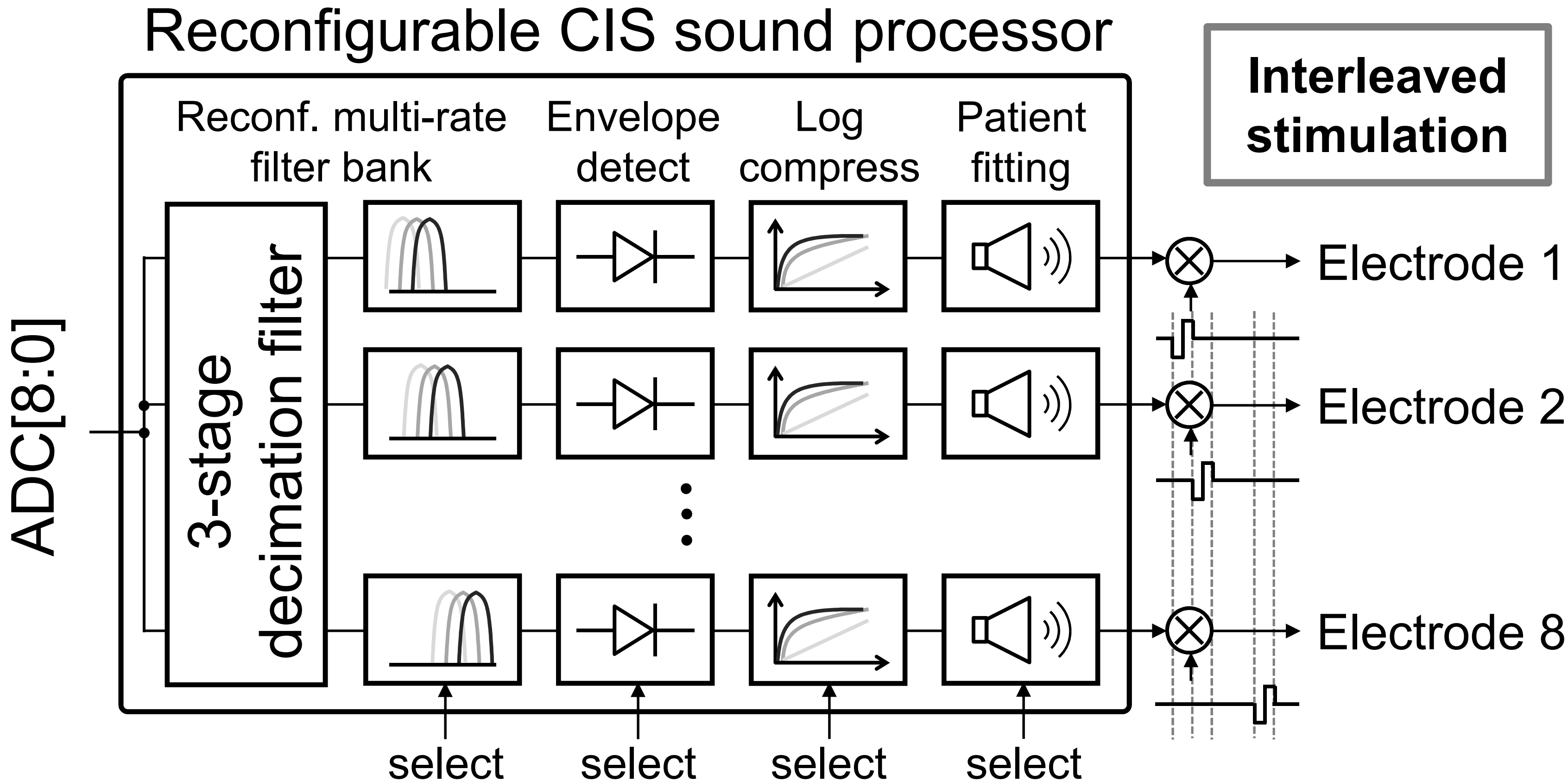
[Yip, *ISSCC*'11]

CIS Sound Processing Strategy



- ***Continuous Interleaved Sampling (CIS)*** sound processing strategy used by a majority of today's cochlear implants
- Interleaved stimulation reduces channel interactions

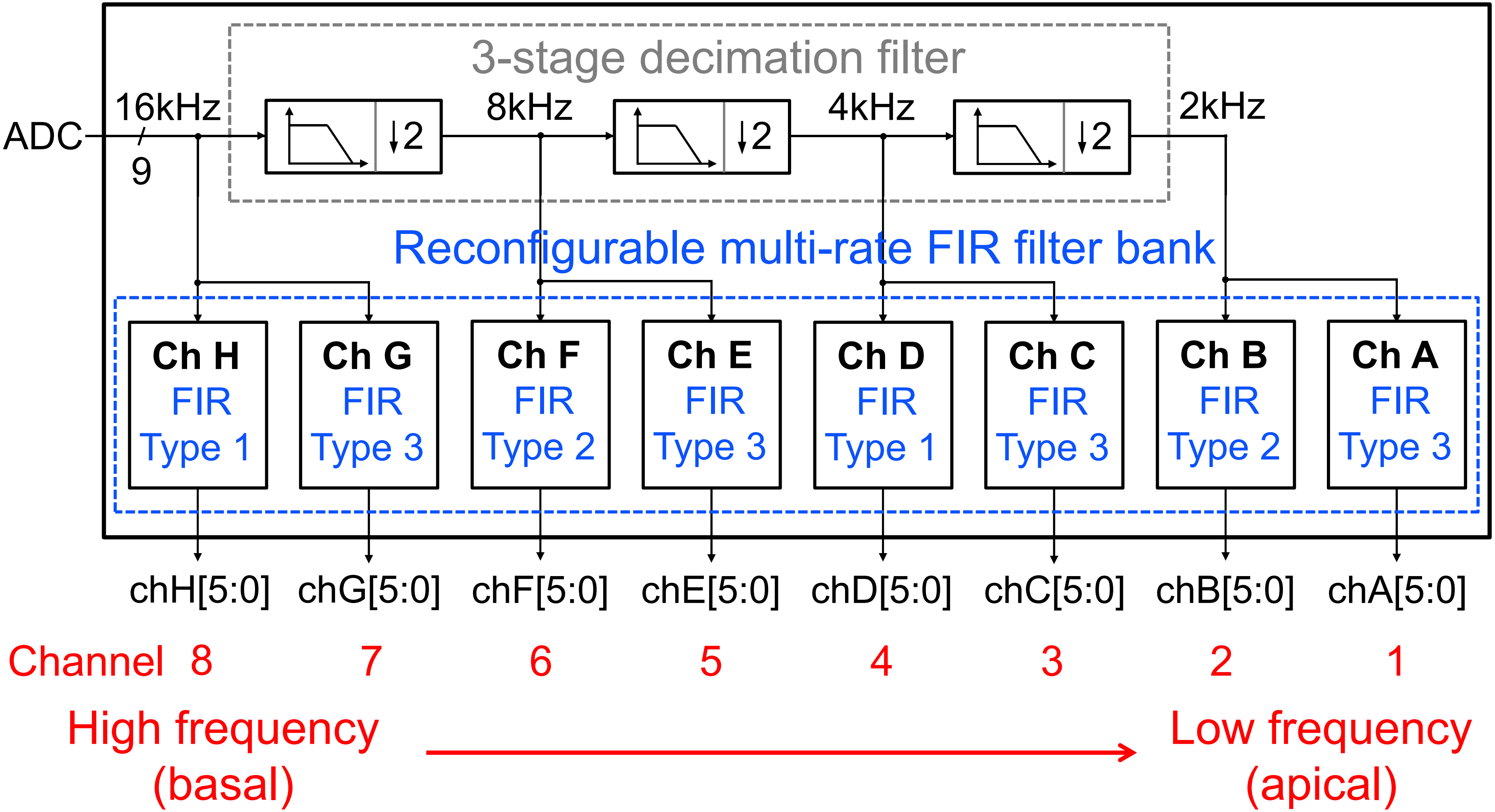
Reconfigurable Sound Processor



- Reconfigurable # of channels (4, 6, 8) for power-performance tradeoff
- Reconfigurable multi-rate FIR filter bank to reduce power and area
- Programmable processor settings (rectification, gain, compression)
- Patient fitting capability (threshold and most-comfortable level)

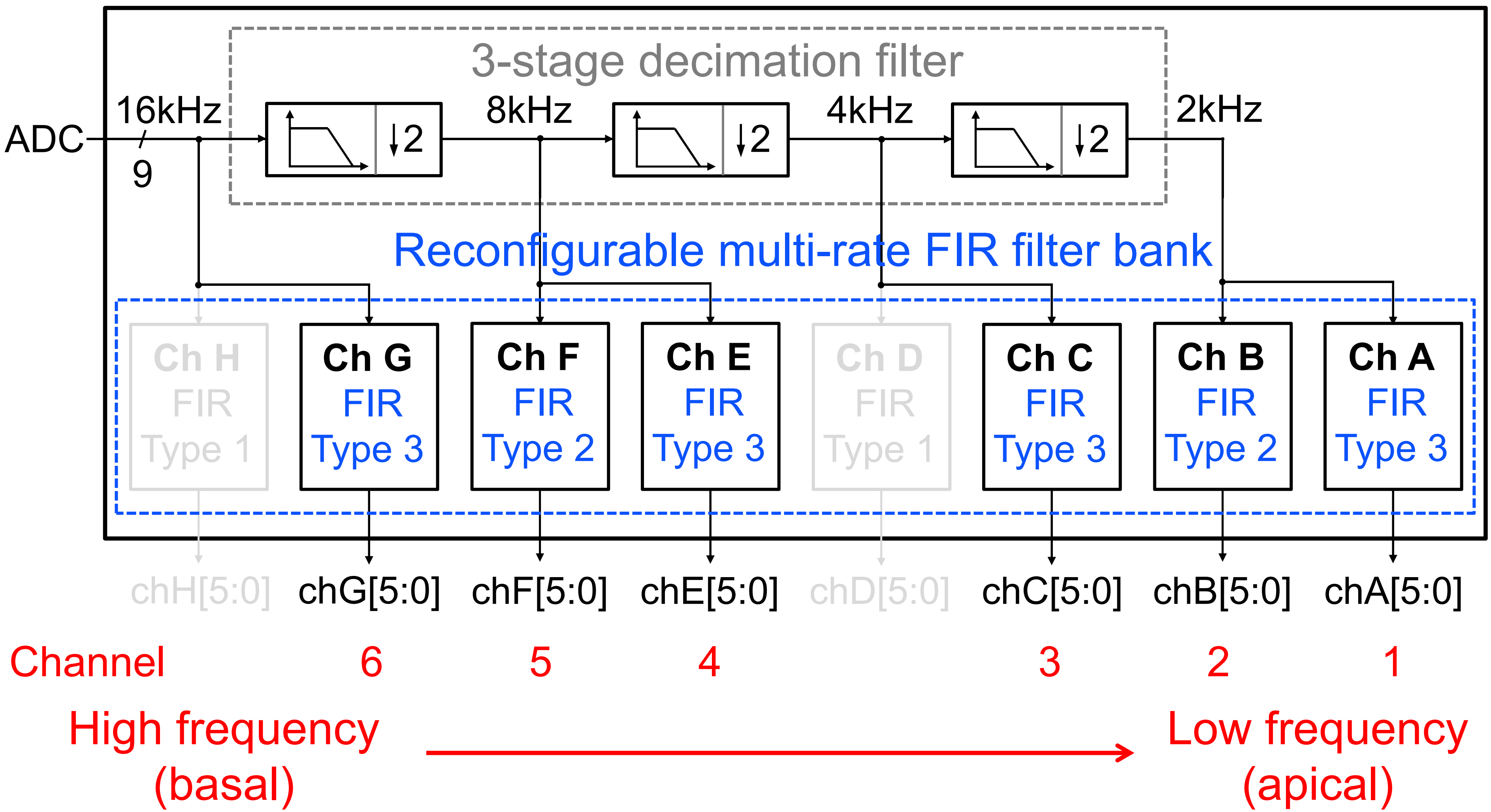
Multi-rate Filter Bank Architecture

8-channel mode

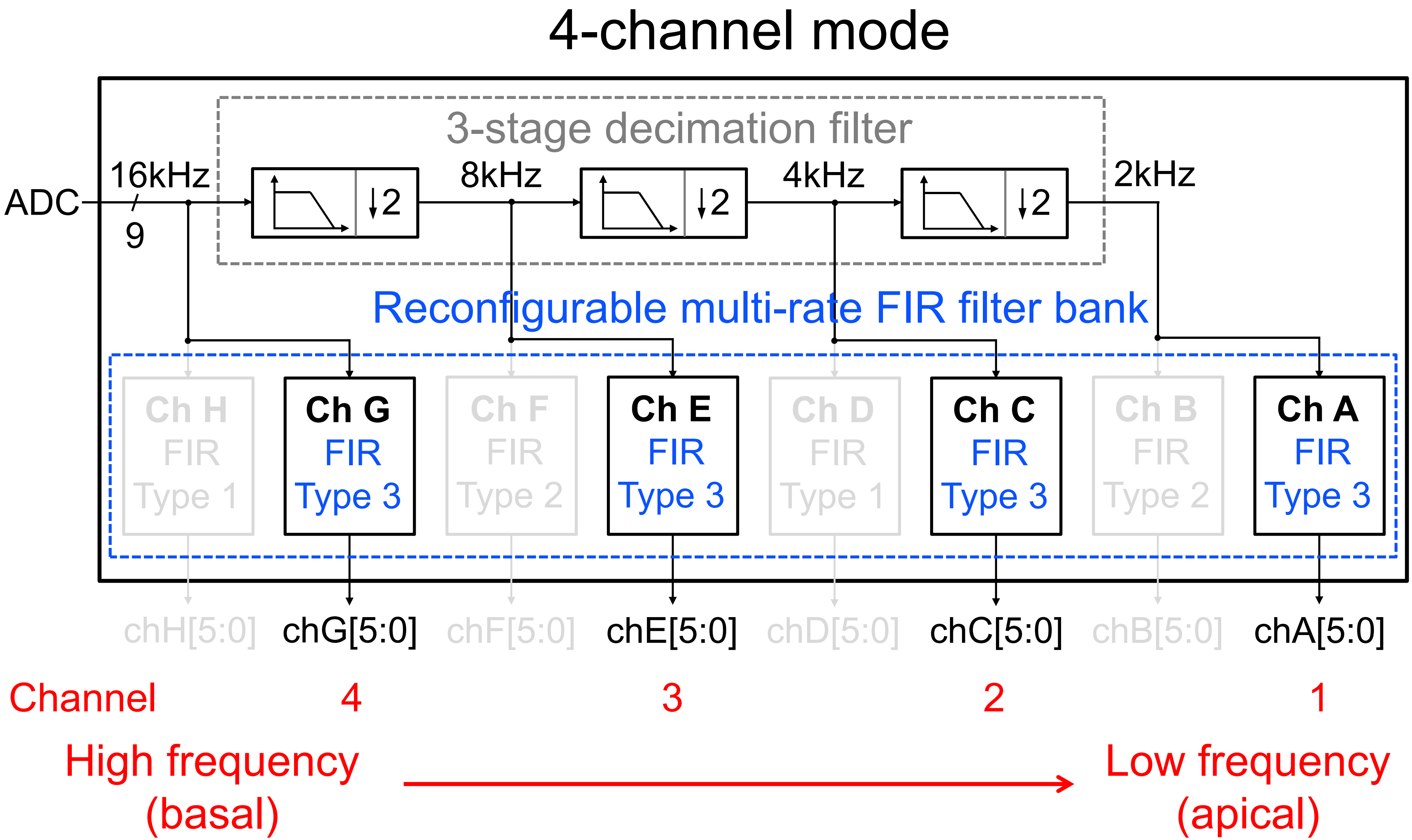


Multi-rate Filter Bank Architecture

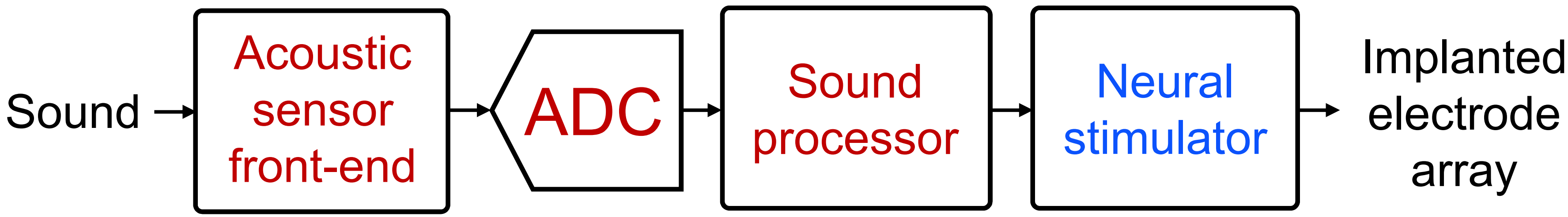
6-channel mode



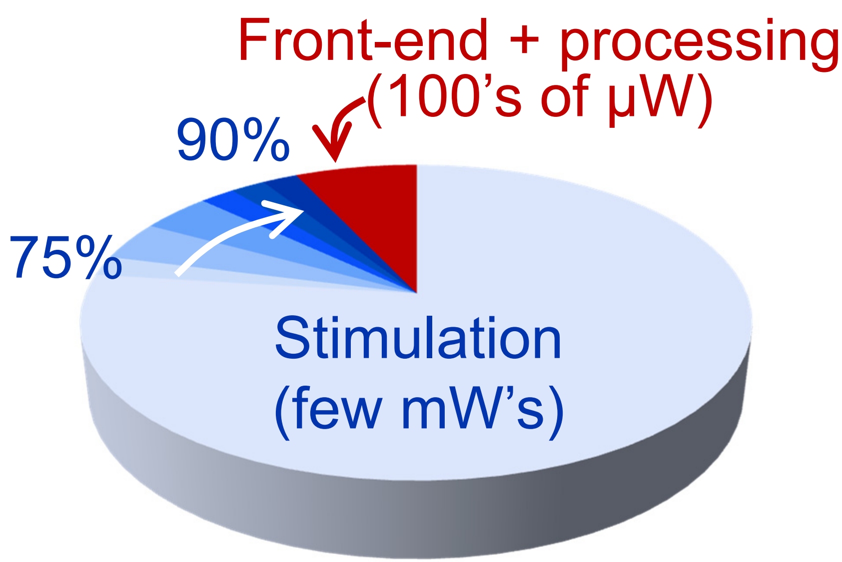
Multi-rate Filter Bank Architecture



CI Power Breakdown



Power breakdown of a fully-implantable CI

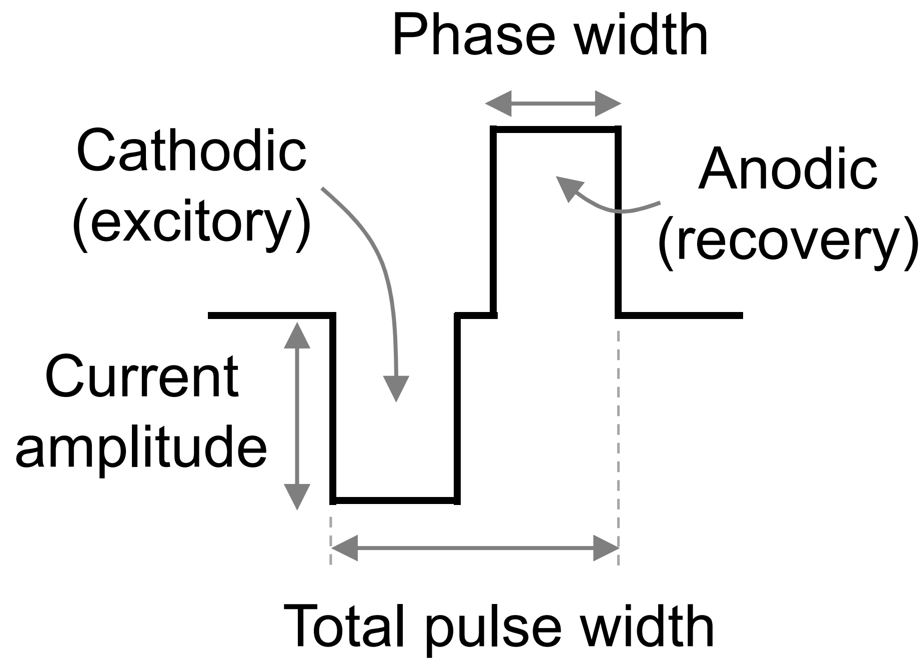


- Stimulation power dominates because of:
  - Threshold for action potential
  - Electrode impedance

Require energy-efficient neural stimulation

Energy-Efficient Stimulation

- Most neural stimulators use charge-balanced rectangular biphasic current pulses
- Alternate stimulation waveforms: lack of consensus and experimental results
- This work: ***neural activation*** is the goal function



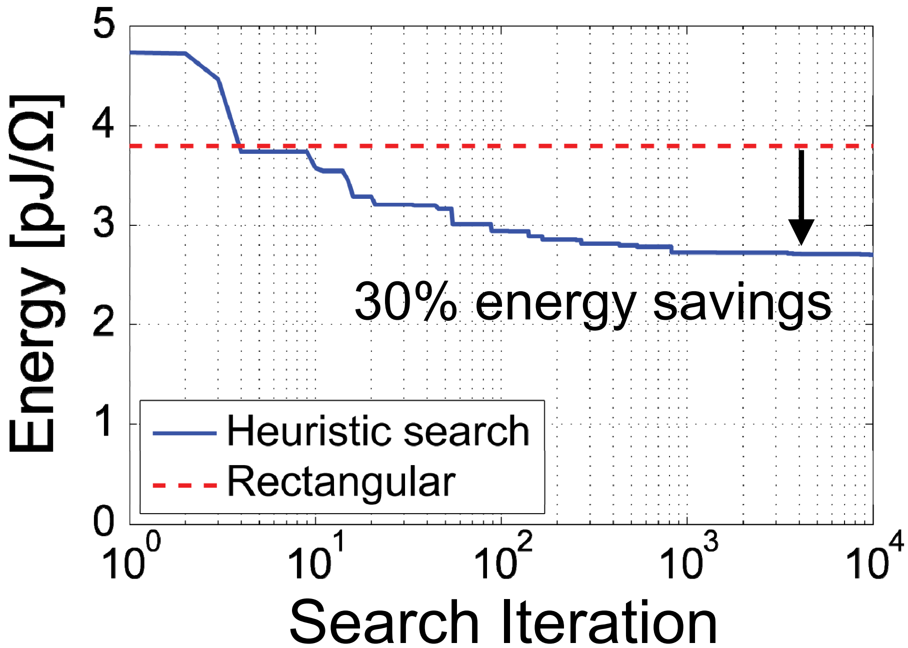
Goals:

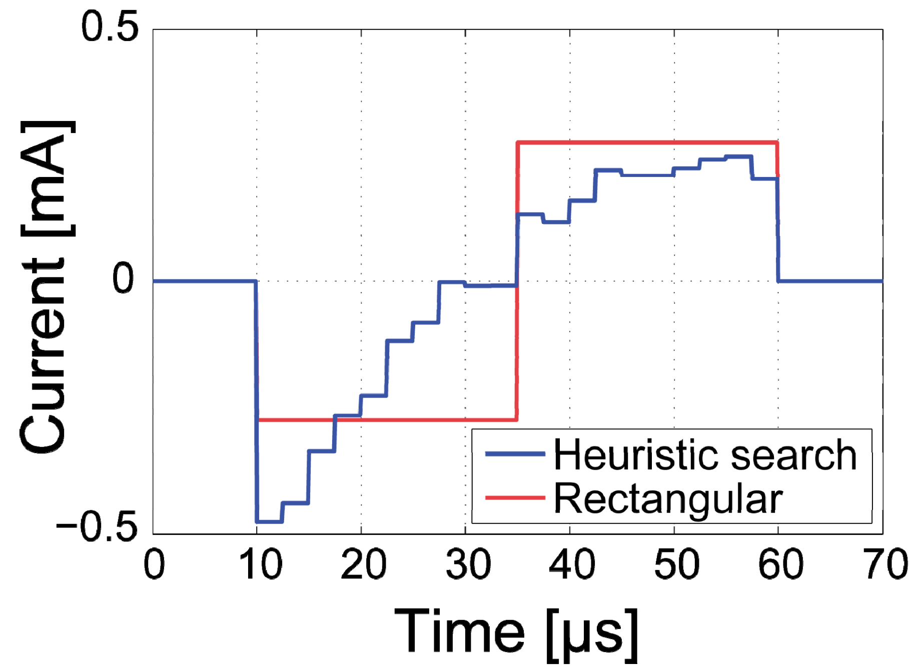
1) Minimize amount of energy for same neural response

2) Experimental validation with in-vivo measurements

Search for Energy-Efficient Stimulation Waveform

- Use heuristic search (based on [1]) with computational auditory nerve fiber model to seek out energy-optimal waveform



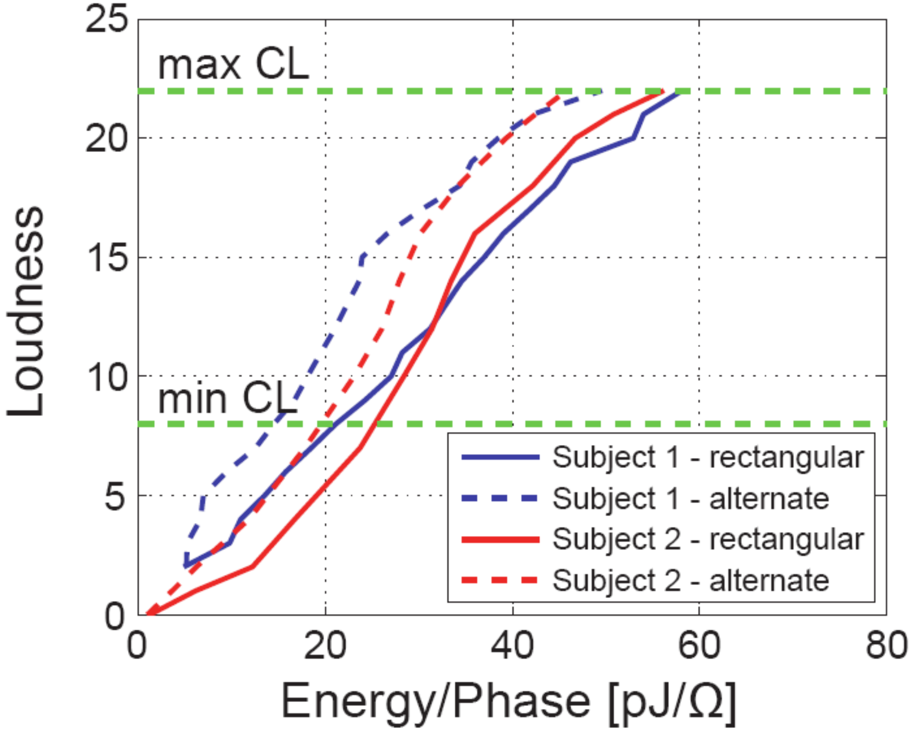


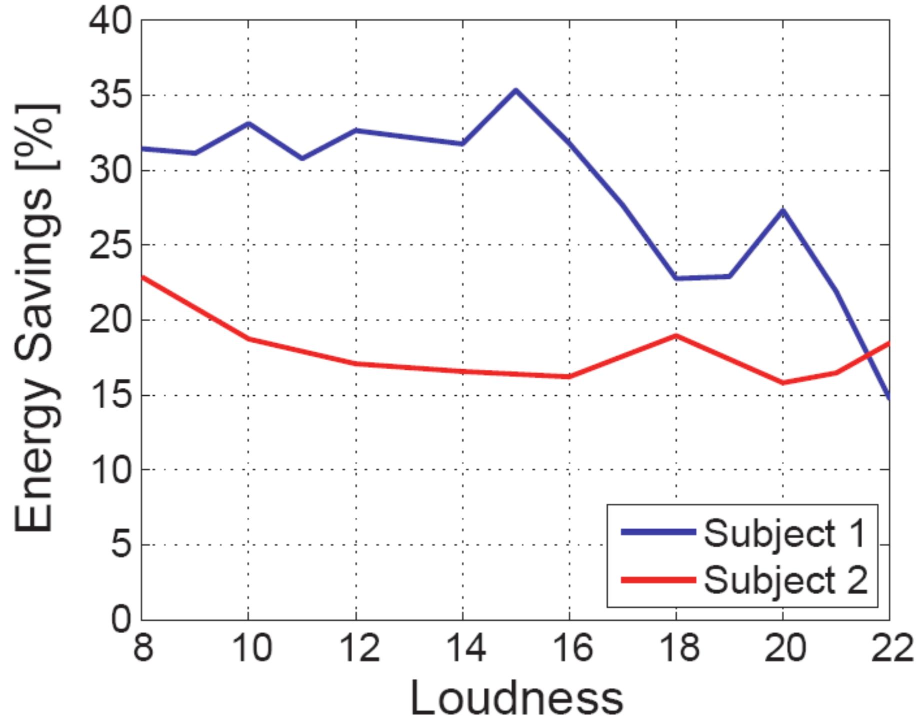
Energy-optimal waveform from computational model is 30% more efficient than rectangular waveform

[1] A. Wongsarnpigoon et al., *Journal of Neural Eng.*, vol. 7, no. 4, Aug. 2010.

Validation with Human Subject Testing

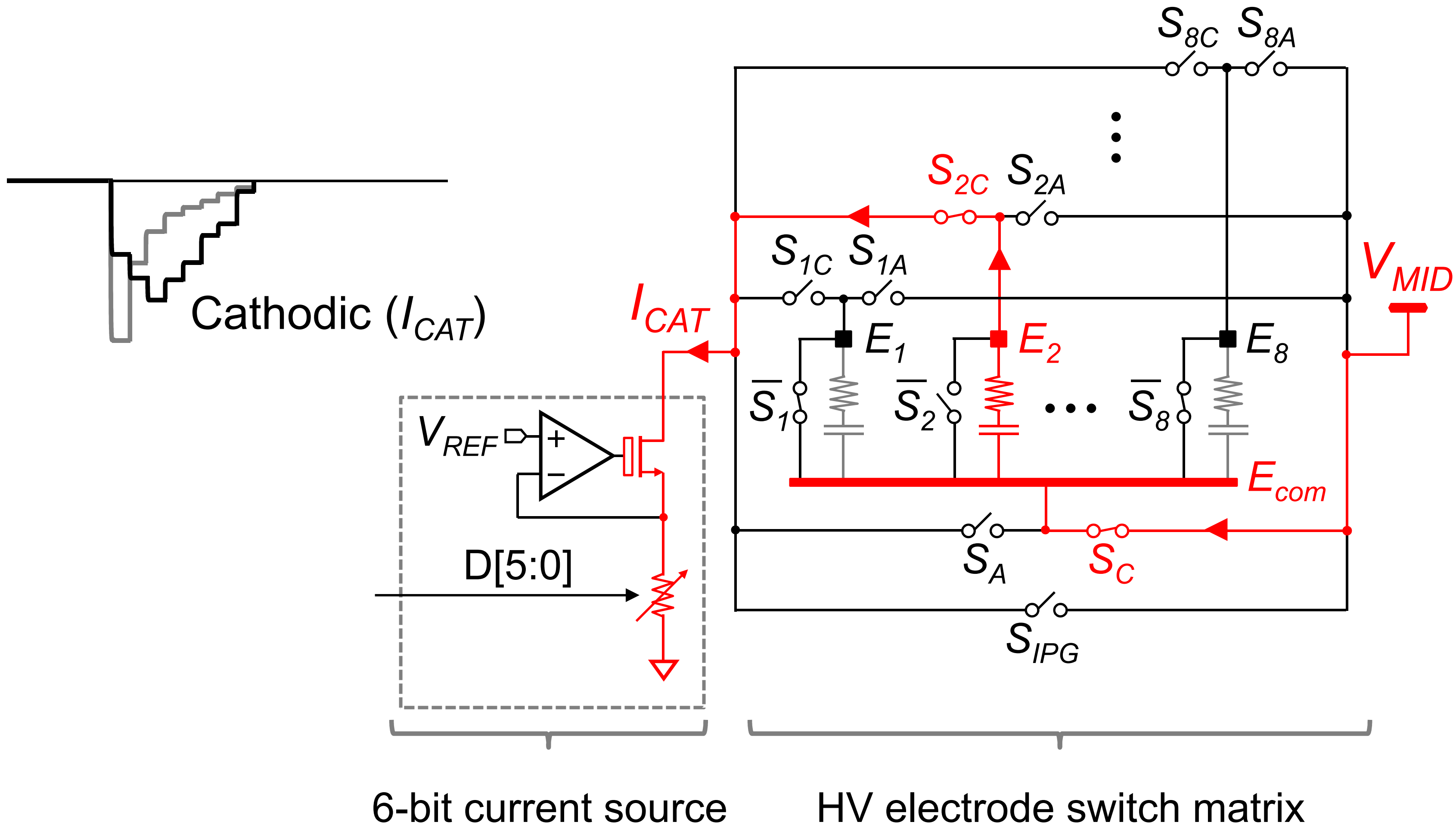
- Loudness perception testing of human CI users show 15% to 30% energy savings





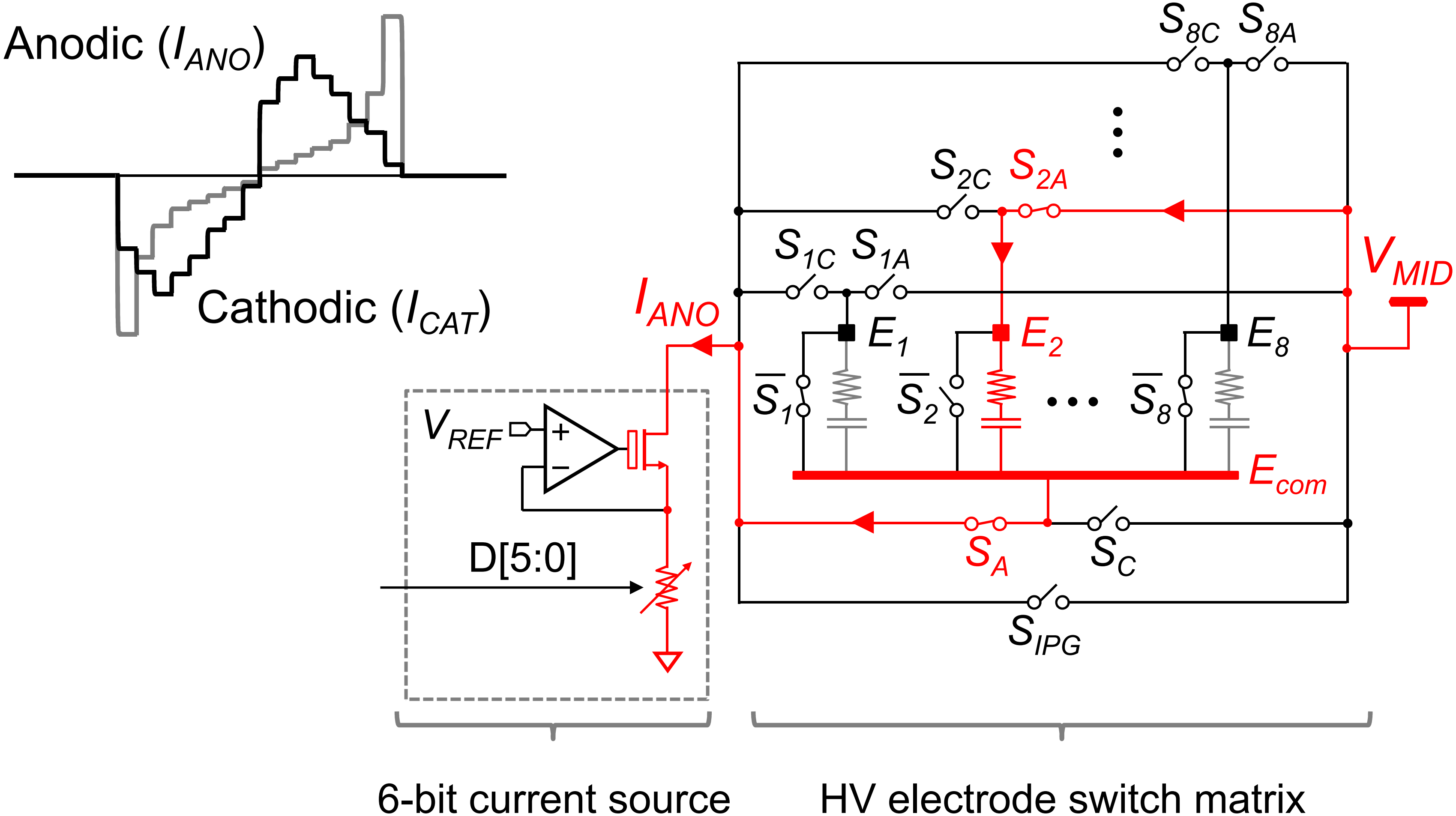
Energy savings from stimulation waveform transfer directly to system

Arbitrary Waveform Stimulator and HV Switch Matrix



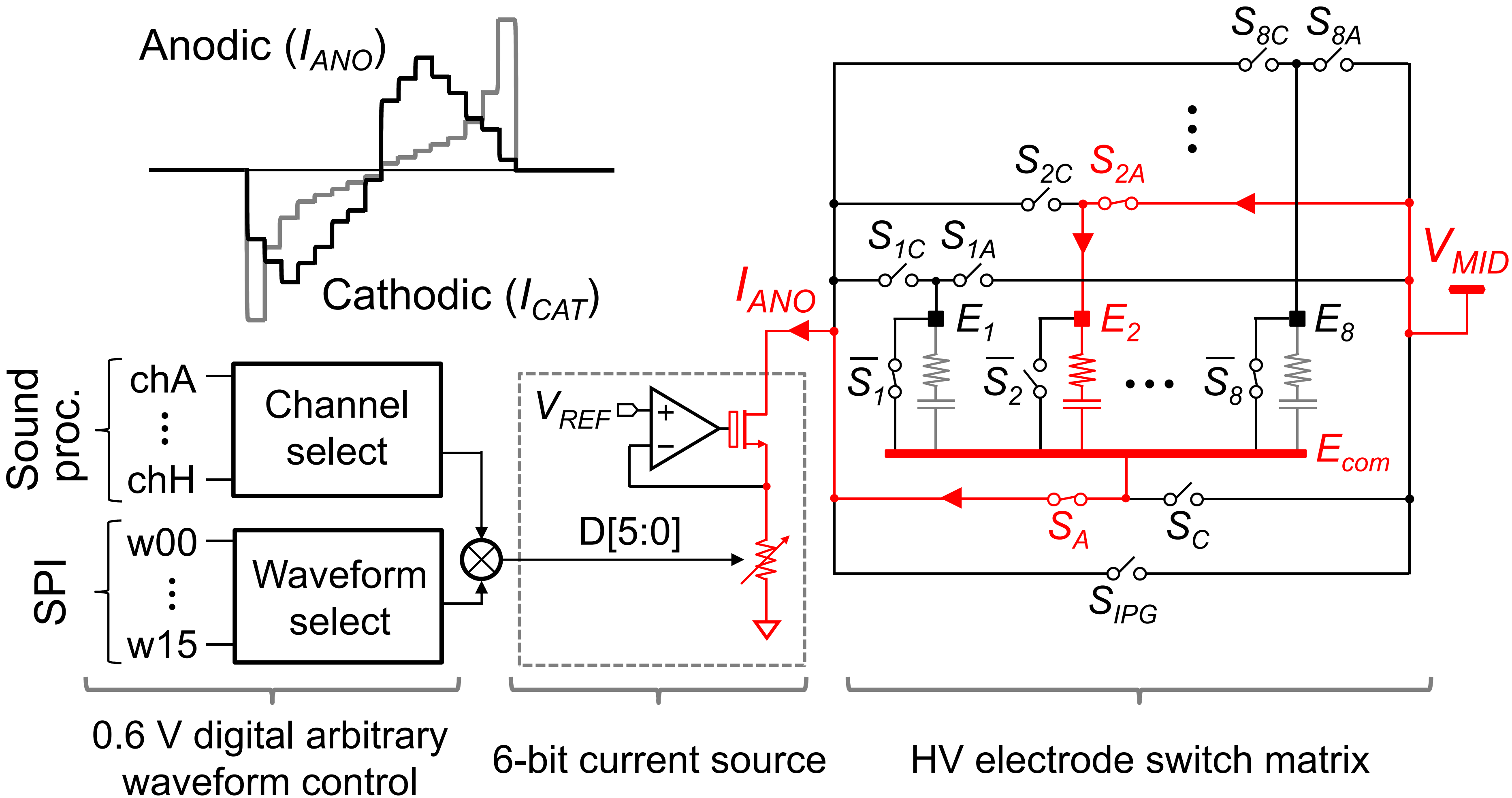
- Single digitally-controlled current source interleaved between all electrodes using switch matrix

Arbitrary Waveform Stimulator and HV Switch Matrix



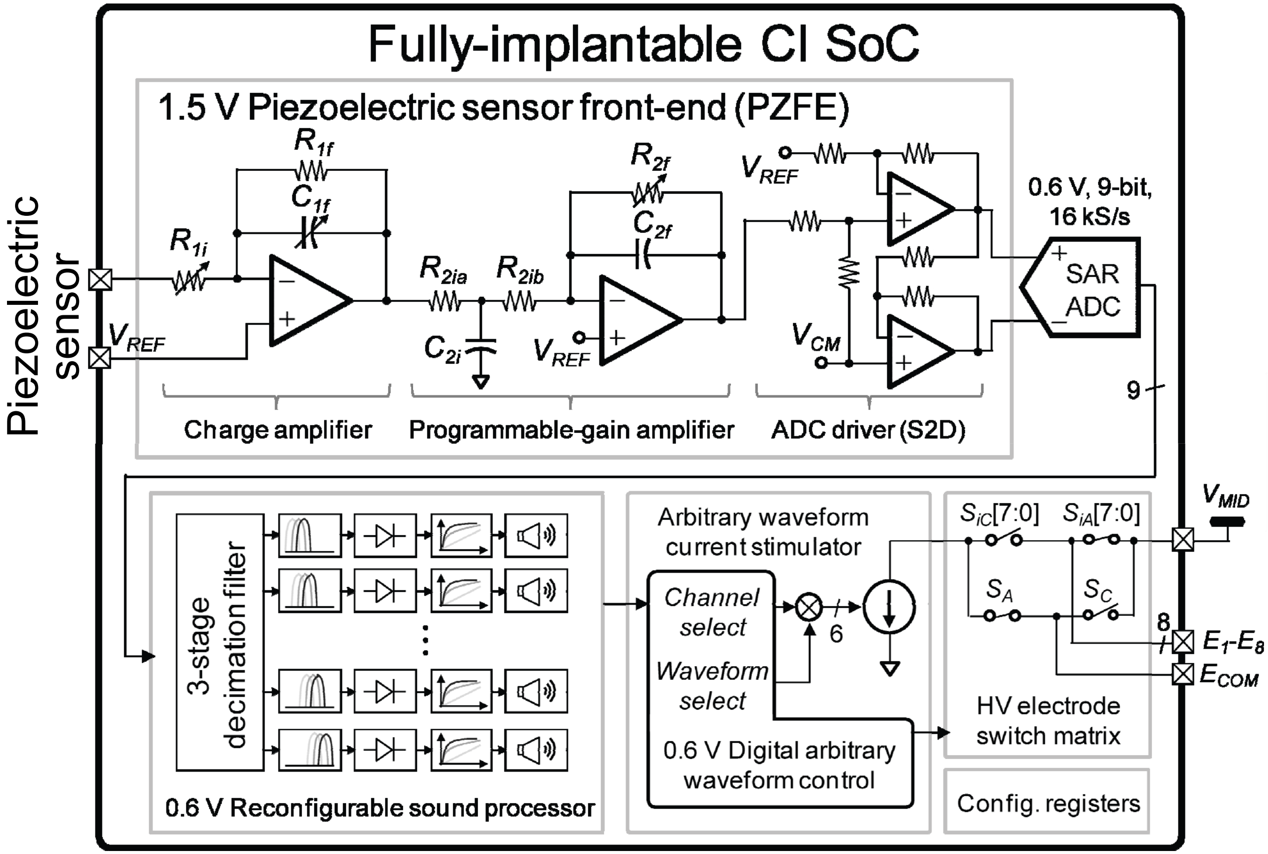
- Single digitally-controlled current source interleaved between all electrodes using switch matrix

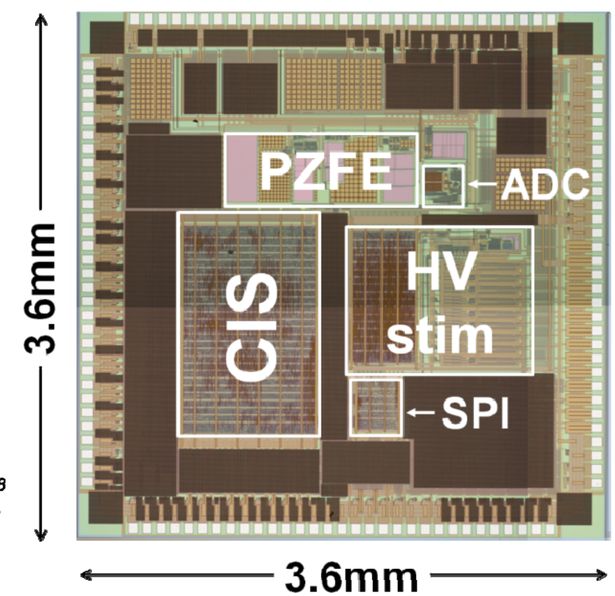
Arbitrary Waveform Stimulator and HV Switch Matrix



- Single digitally-controlled current source interleaved between all electrodes using switch matrix

Fully-Implantable CI Prototype

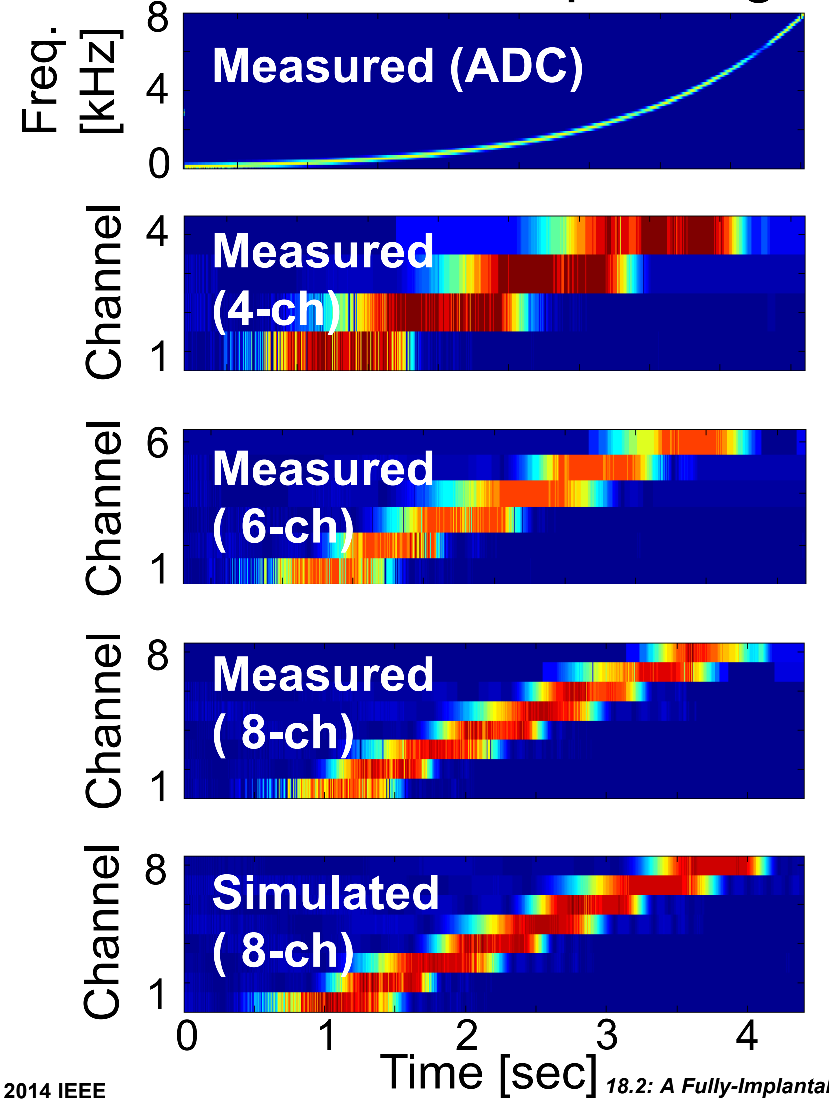




Prototyped in 0.18µm HV CMOS

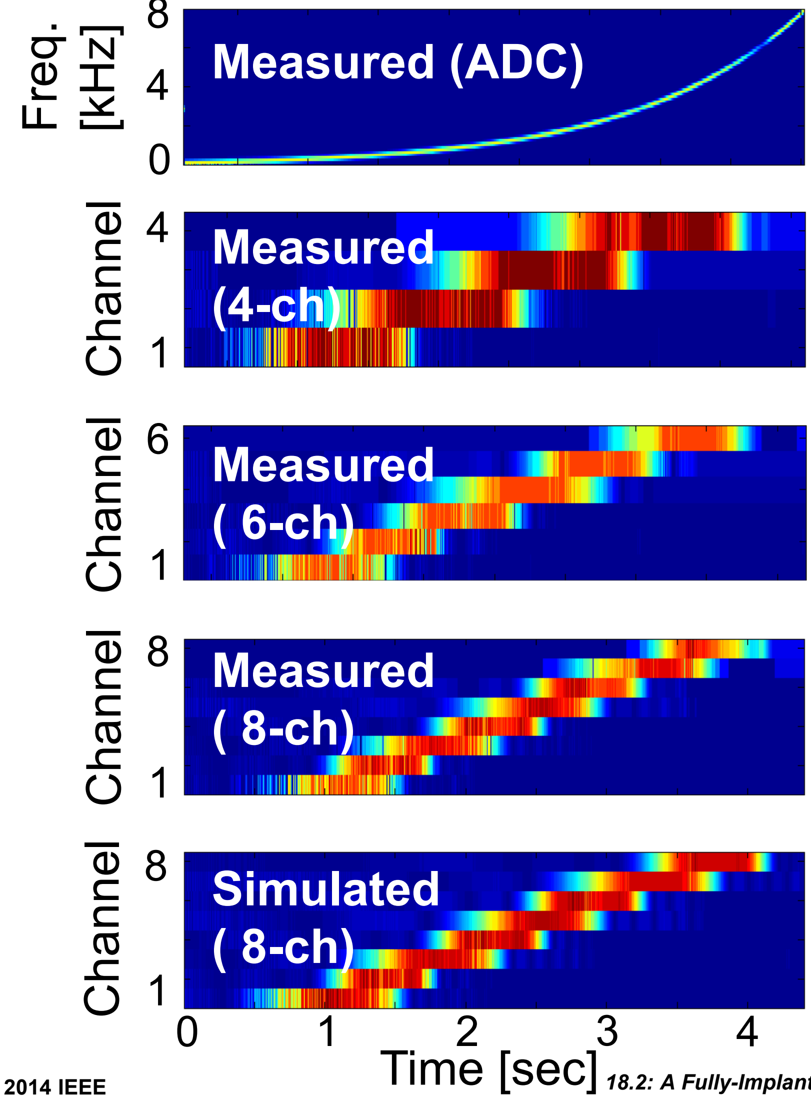
Reconfigurable CIS Sound Processor

- Reconstructed spectrograms with log-chirp input at ADC

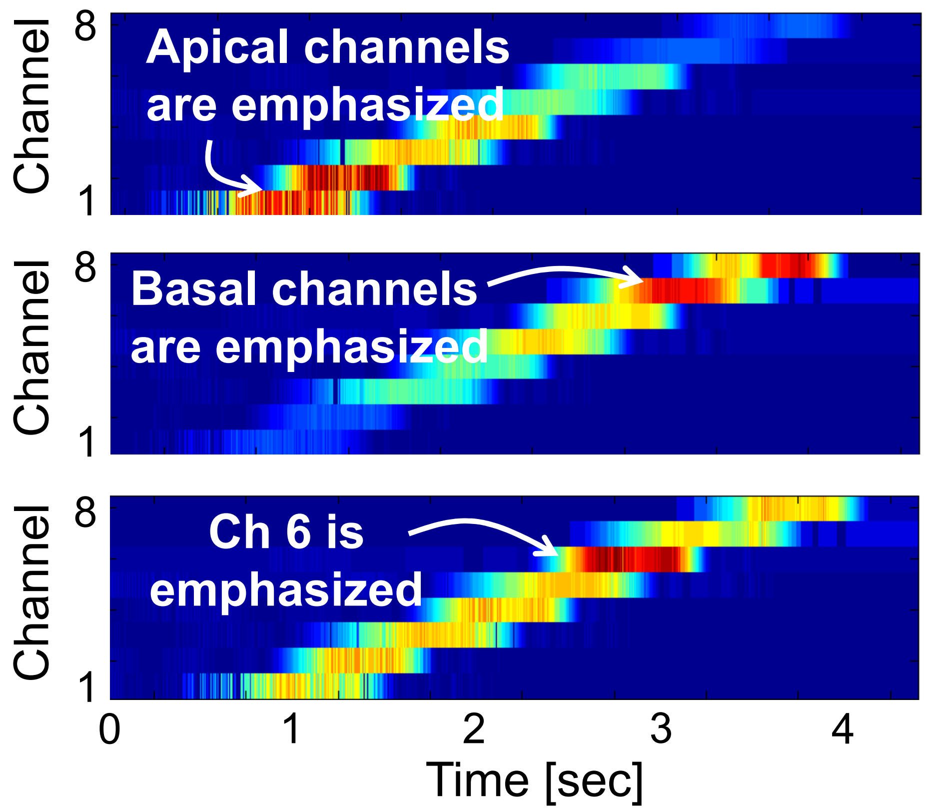


Reconfigurable CIS Sound Processor

- Reconstructed spectrograms with log-chirp input at ADC



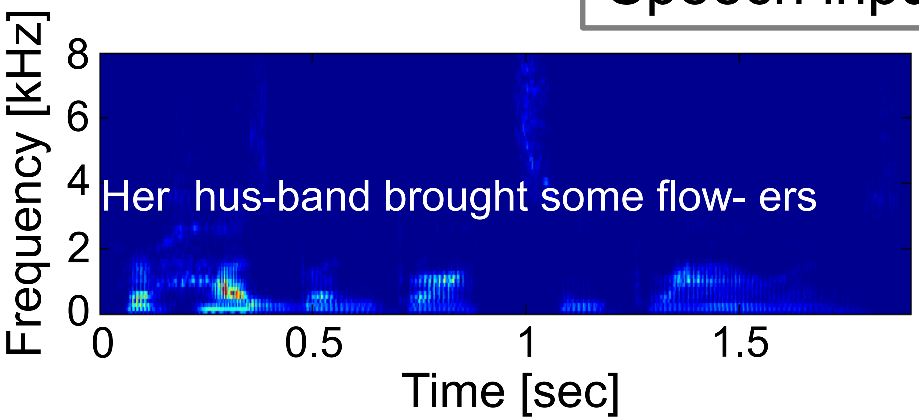
Patient fitting capability

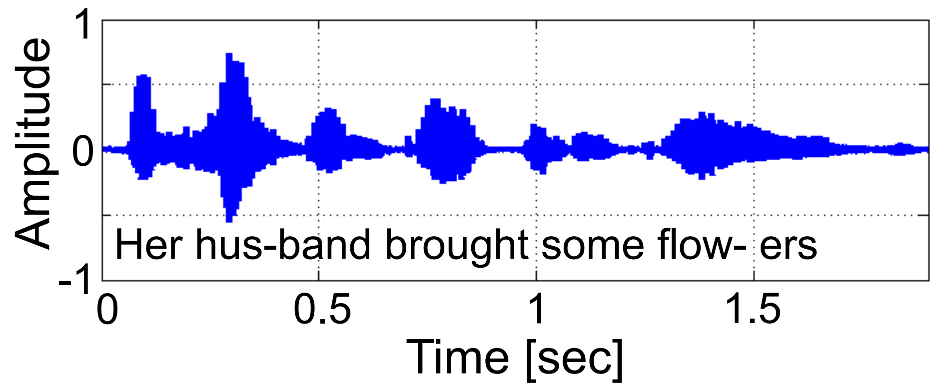


System Demo with Human Cadaveric Specimen

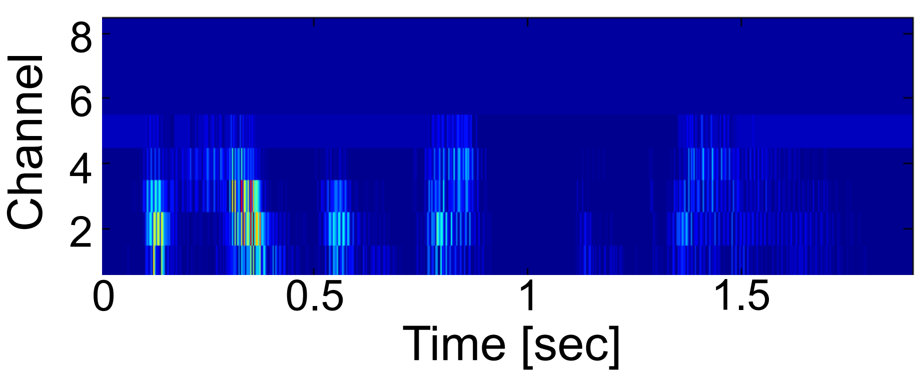
- Speech clip played into human cadaveric middle ear
- Measured signal chain includes PZFE + ADC + CIS processor

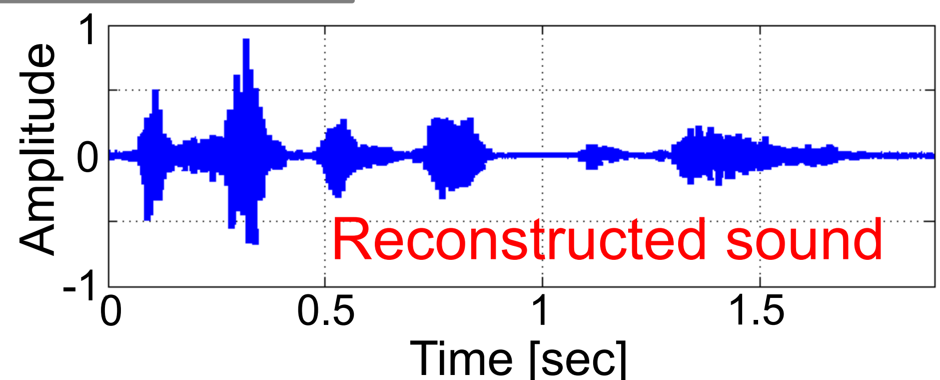
Speech input in ear canal





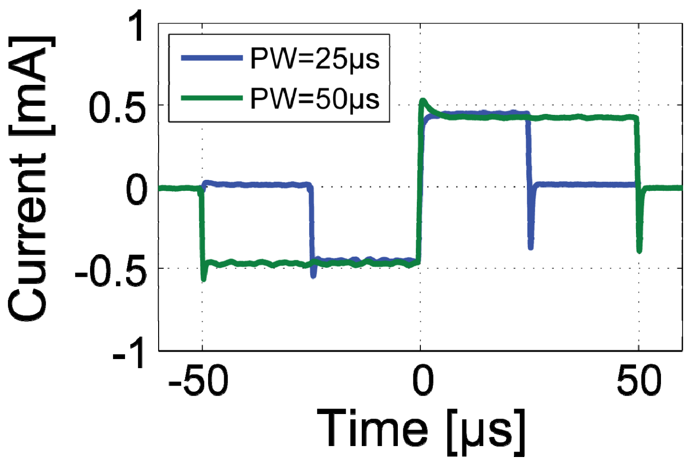
Measured SoC output



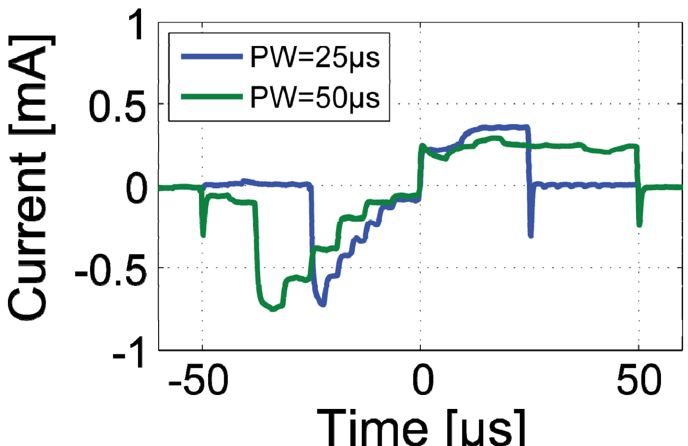


Arbitrary Stimulation Waveforms

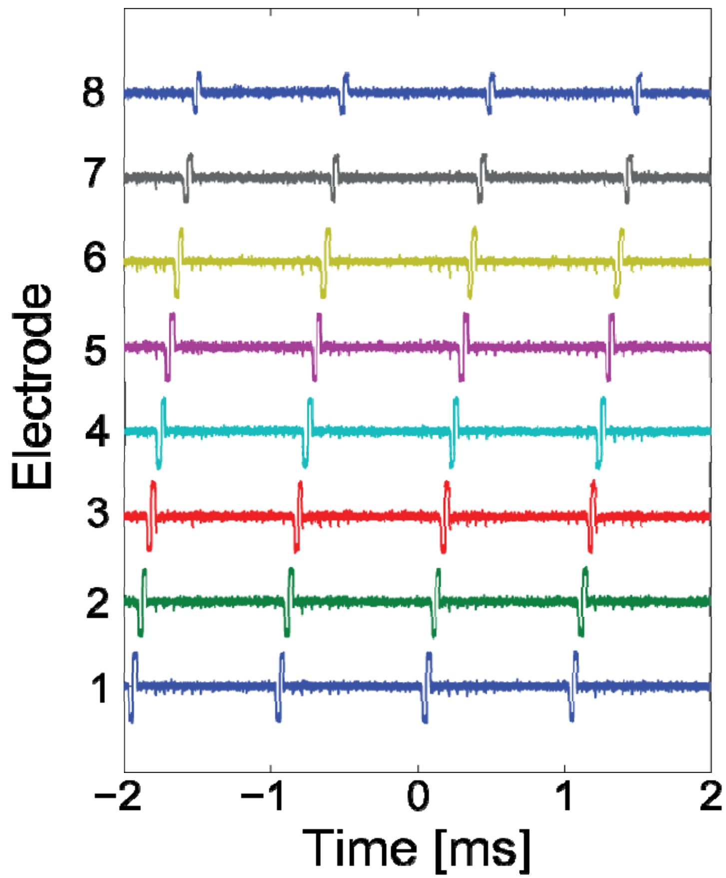
Rectangular waveform



Optimal waveform

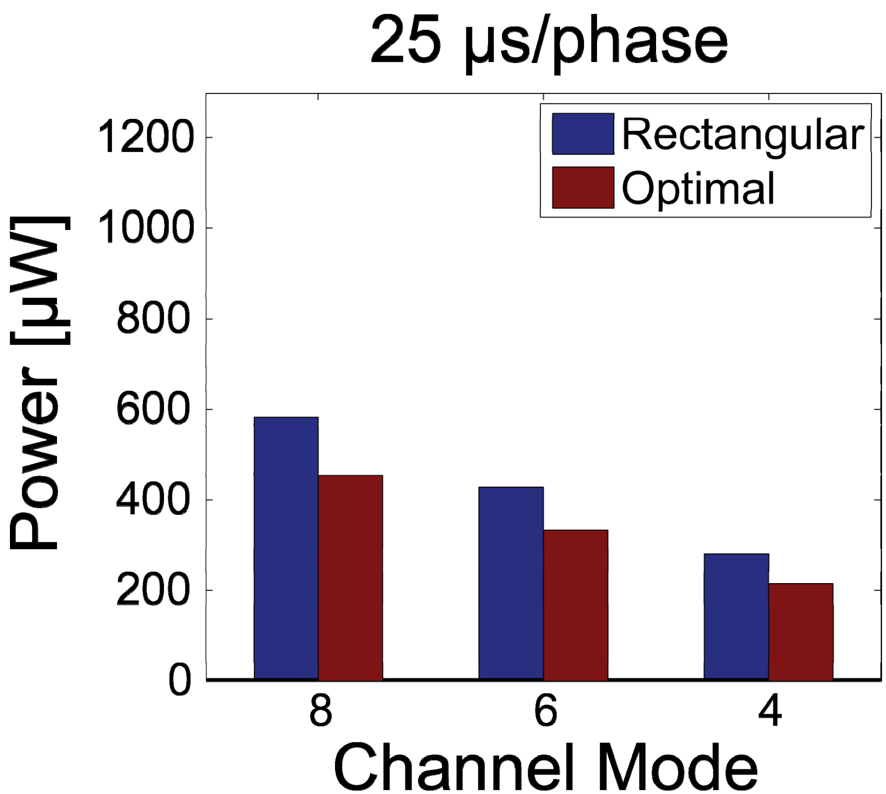


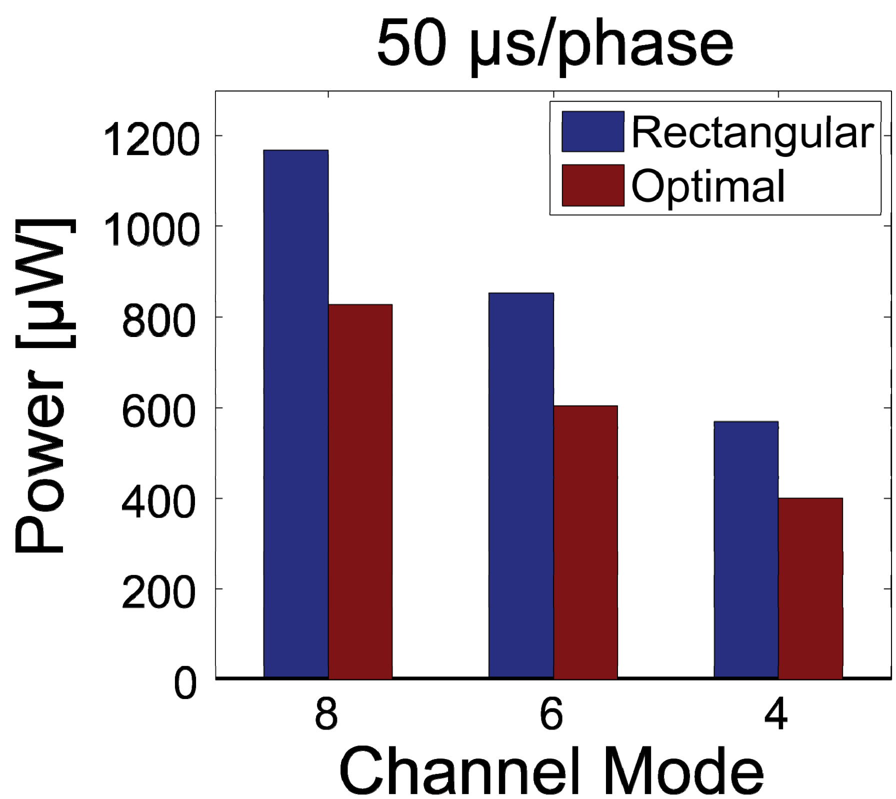
8-electrode array



Neural Stimulation Power

- Measured stimulation power during speech
- Optimal waveform is 29% more efficient at 50 µs/phase





Total CI SoC Power (8-channel)

- Measured power during normal speech with the optimal waveform at phase width = 31.25 μs

Block	Supply voltage [V]	Supply current [μA]	Power [μW]	% of total power
PZFE	1.5	6.8	10.3	**1.8%**
SAR ADC (9-bit, 16 kS/s)	0.6	0.5	0.3	**0.05%**
Digital CIS sound processor	0.6	2.7	1.6	**0.28%**
Stimulator and switch matrix			560	**97.9%**
Digital waveform interface	0.6	0.6	0.4	0.07%
Level shifters	1.8	0.2	0.4	0.07%
Current source circuits	3.3	22.7	74.9	13%
Stimulator supply (5V to 10V)	7	68.4	479	84%
Switch matrix (7V to 12V)	9	0.6	5.4	0.9%
Total CI SoC (8-channel mode)			572	100%

Summary of Fully-Implantable CI

- Prototype of fully-implantable CI SoC implemented in 0.18µm HV CMOS
  - Feasibility of middle-ear piezoelectric sensor as an implantable acoustic sensor
  - ULP reconfigurable CIS sound processor
  - Alternate (non-rectangular) stimulation waveforms are more energy-efficient

Acknowledgements:

- NSERC Fellowship, Bertarelli Foundation, TSMC University Shuttle
- Don Eddington, Victor Noel, Ken Hancock, Dave Perreault

A Multi-Parameter Signal-Acquisition SoC for Connected Personal Health Applications

Nick Van Helleputte[1], Mario Konijnenburg[2], Hyejung Kim[1], Julia Pettine[2], Dong-Woo Jee[1], Arjan Breeschoten[2], Alonso Morgado[1], Tom Torfs[1], Harmke de Groot[2], Chris Van Hoof[2], Refet Firat Yazicioglu[2]

[1]imec, Leuven, Belgium
[2]imec – Holst Centre, Eindhoven, The Netherlands

Holst Centre
Open Innovation by IMEC and TNO

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- Motivation

- Architecture
- Instrumentation amplifier
- Bio-impedance readout
- Accelerator for vector and matrix operations

- Experimental results
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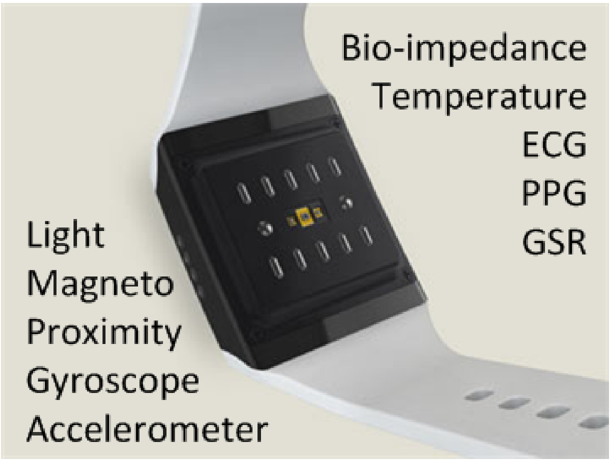
Connected Personal Health

Personal Devices

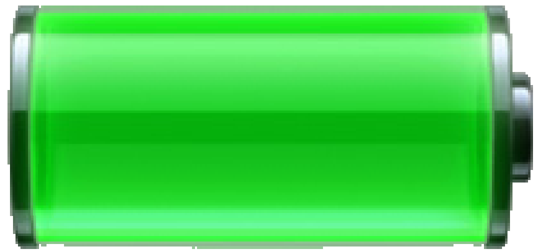
Managing, checking monitoring

KEY CHALLENGES

#1 MULTI-SENSOR

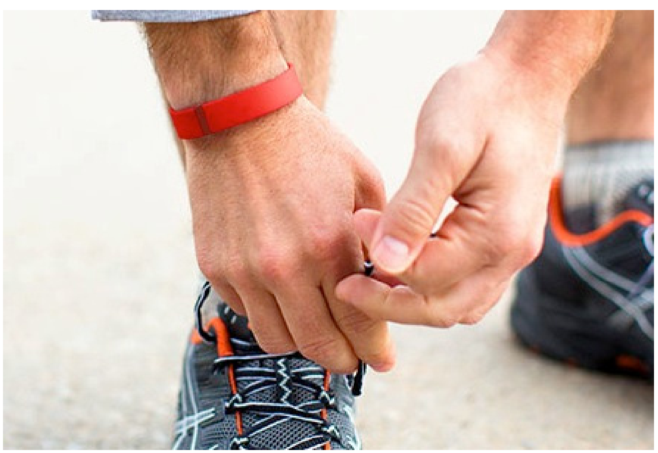


#2 LOW POWER



#3 HIGH QUALITY OF DATA

#4 SMALL FORMFACTOR



#5 LOW COST

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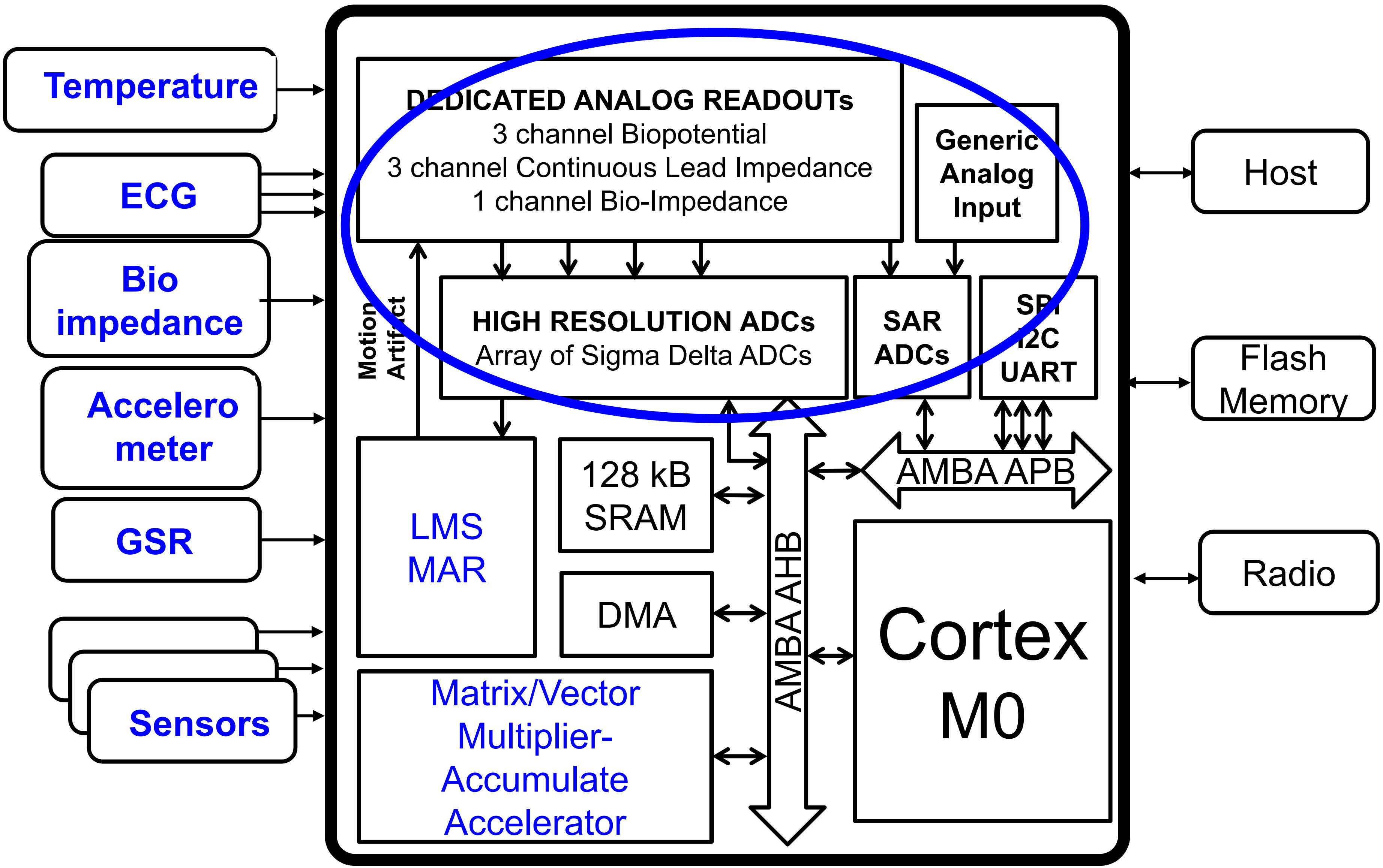
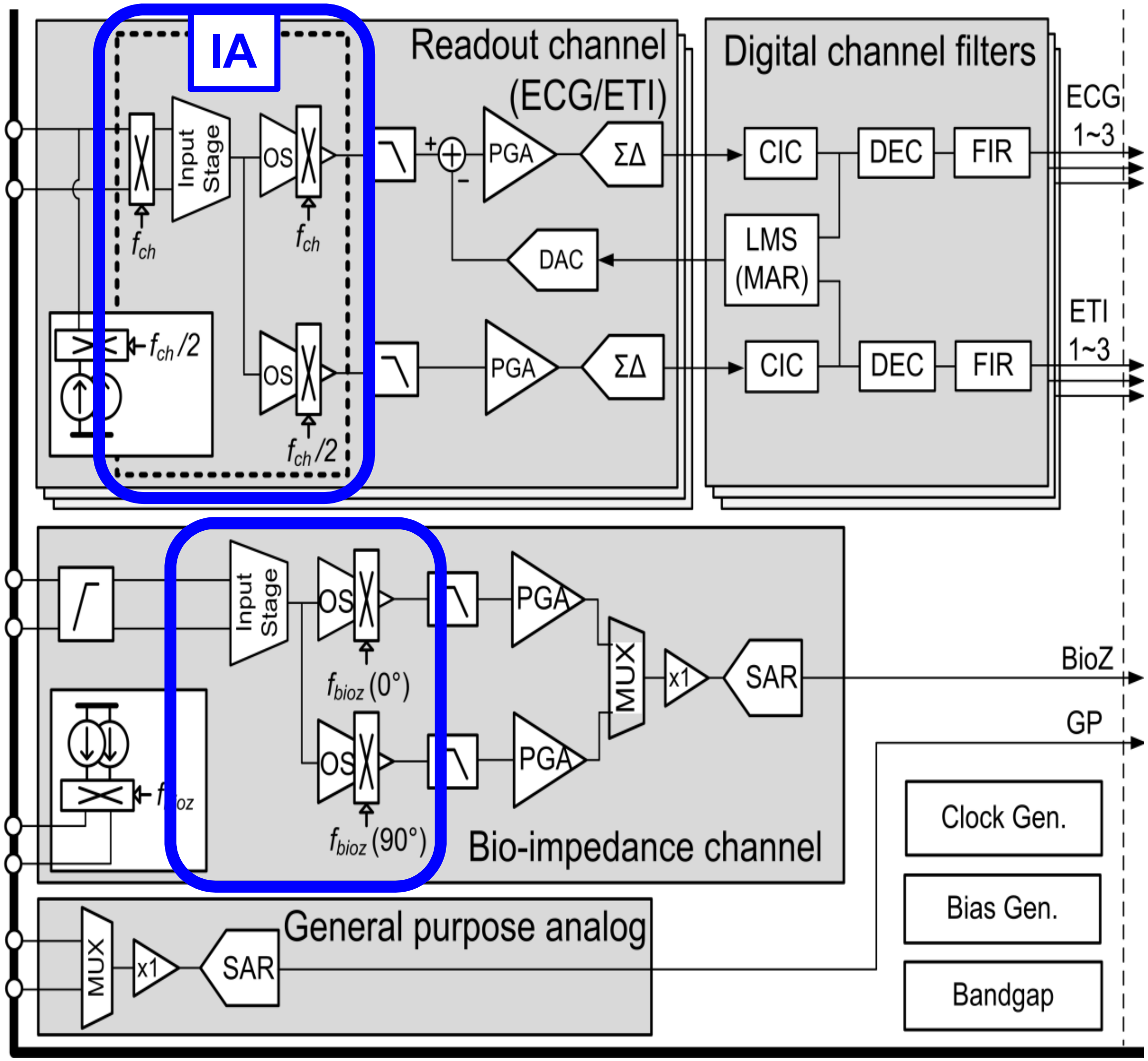
System Architecture



Analog Front-End architecture



- **3 ECG**
  - ECG + concurrent ETI
  - On-chip ΣΔ-ADCs
  - Fully integrated real-time MAR
  - **High-performance IA**
- **Bio-Impedance**
  - Pseudo-sine current source
  - **High-performance IA**
  - On-chip time-multiplexed SAR-ADC
- **General analog**
  - E.g. temperature sensor, strain sensor, ..

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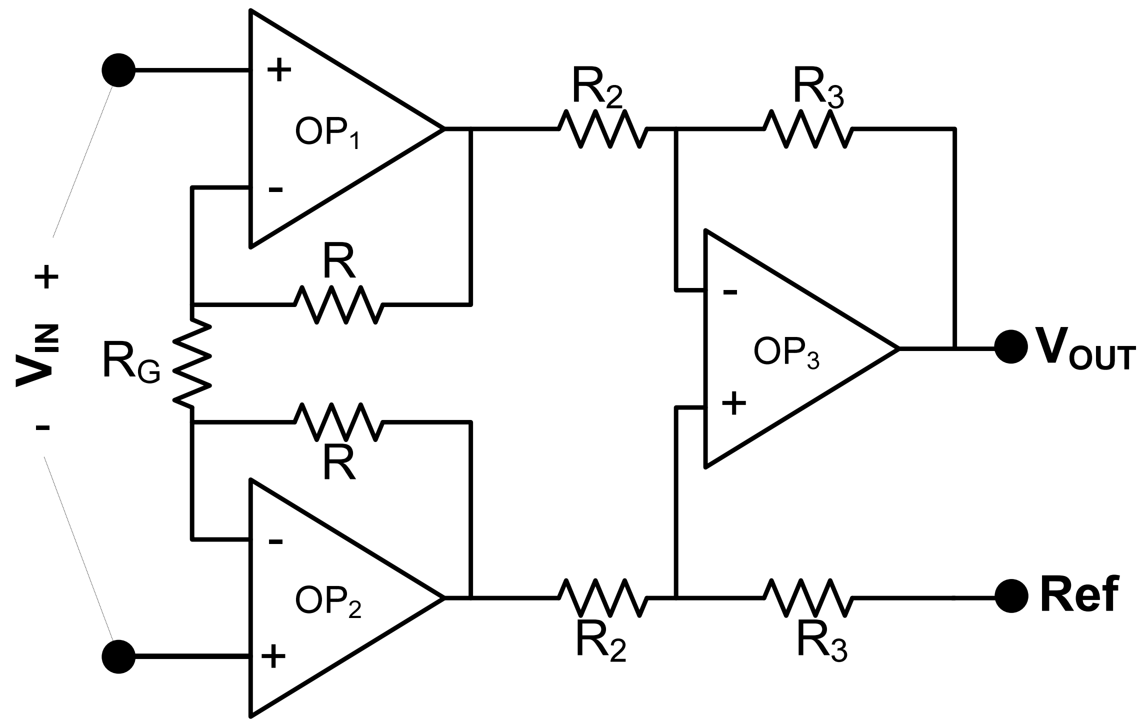
IA design challenges

- **Wearable devices**
  → Highly integrated solution required
  → Low power

- **High signal quality**
  → Low noise
  → High input impedance
  → Large CMRR

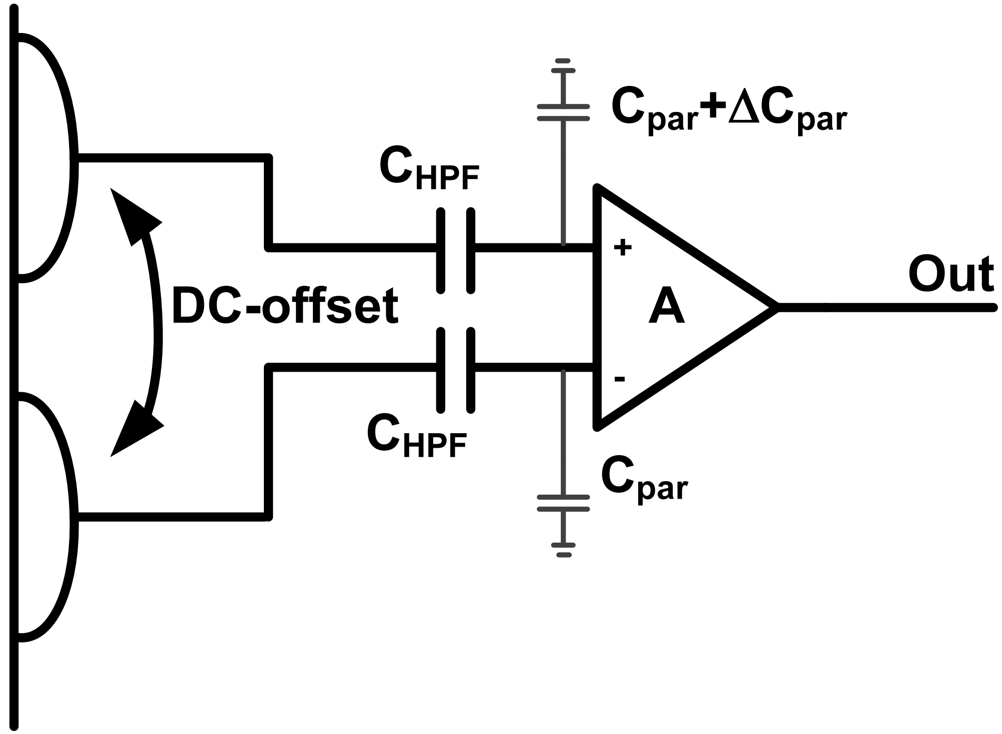
- **Robust operation**:
  i.e. ambulatory conditions lead to motion artifacts (MA)
  → Large dynamic range to avoid saturation due to artifacts
  → Handle large electrode induced DC-offsets

Existing IA shortcomings



- Classic approach (three-opamp IA)
  - No DC offset rejection
  - Low front-end gain puts strict noise requirements on subsequent blocks
  - High power

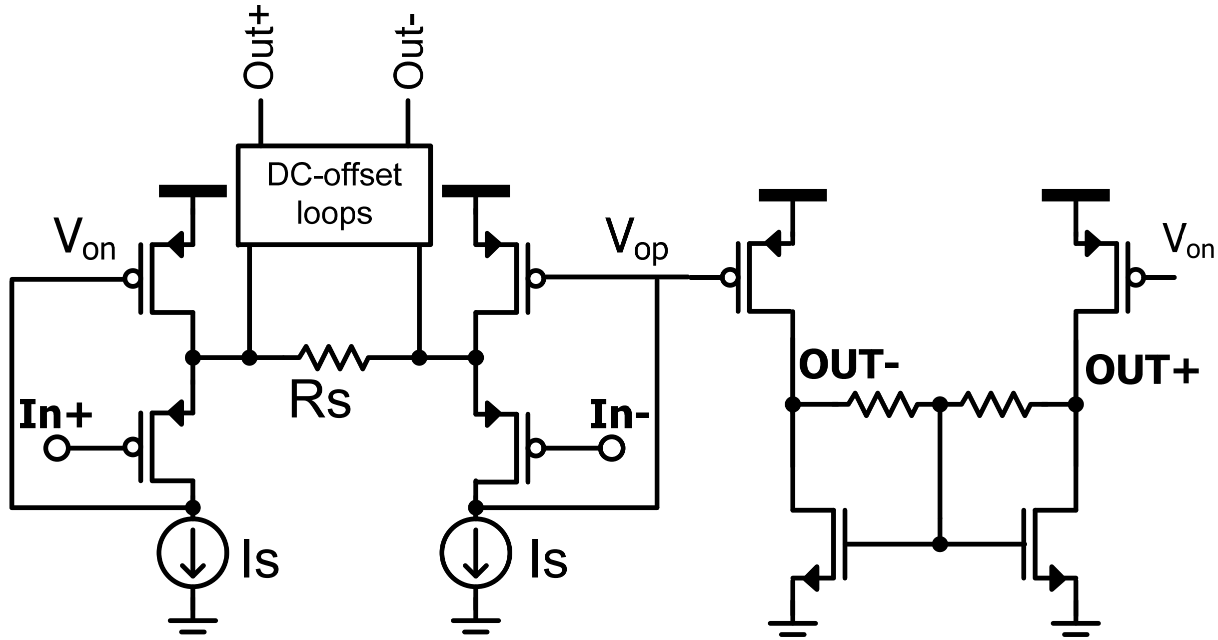
Existing IA shortcomings



$$CMRR \approx \frac{C_{HPF}}{\Delta C_{par}}$$

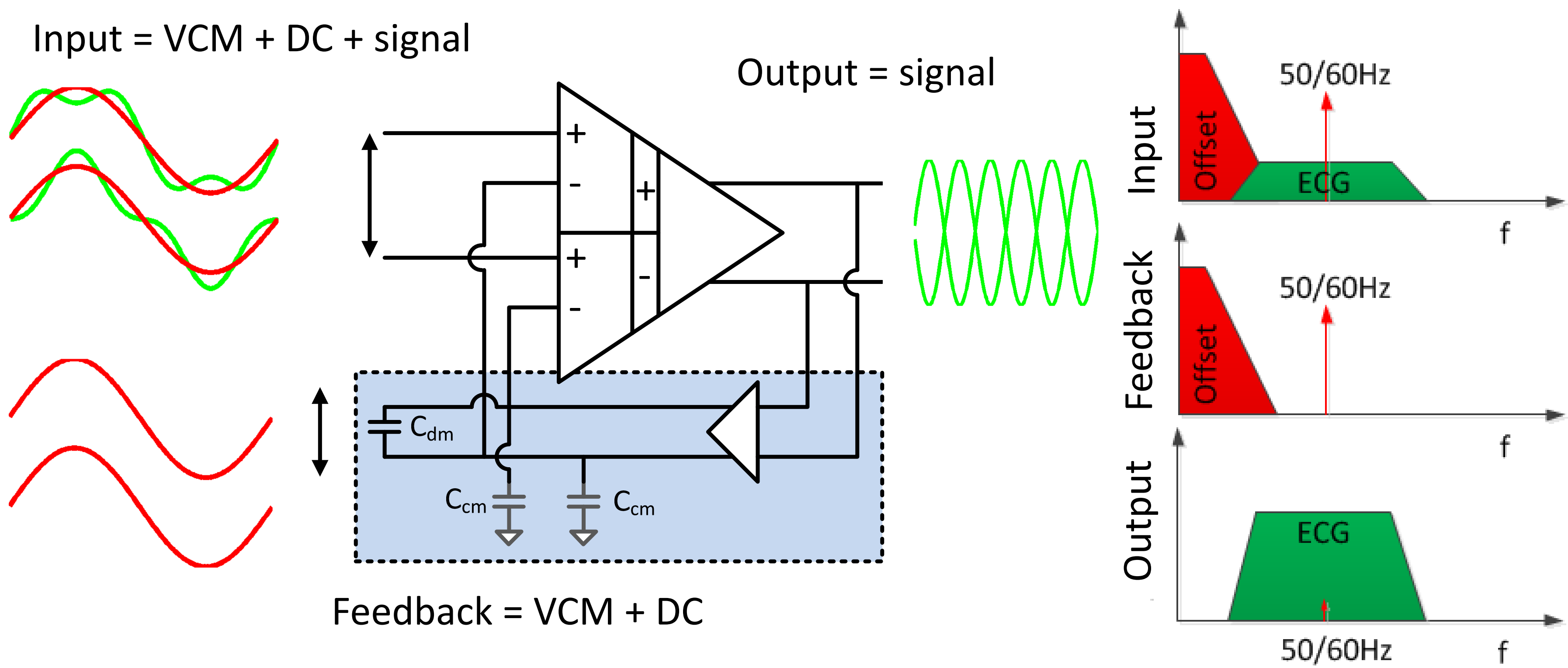
- AC-coupled structures
  - Limited CMRR (cap mismatch)
  - Kt/C noise
  - Often requires external components to achieve good performance (noise/CMRR)

Existing IA shortcomings



- Current-feedback IA (CFBIA)
  - DC-servo can handle limited DC-offset only
    → DC_max = Is * Rs
    → Large DC offset results in operating point mismatch
    → DC-offset reduces usable input signal

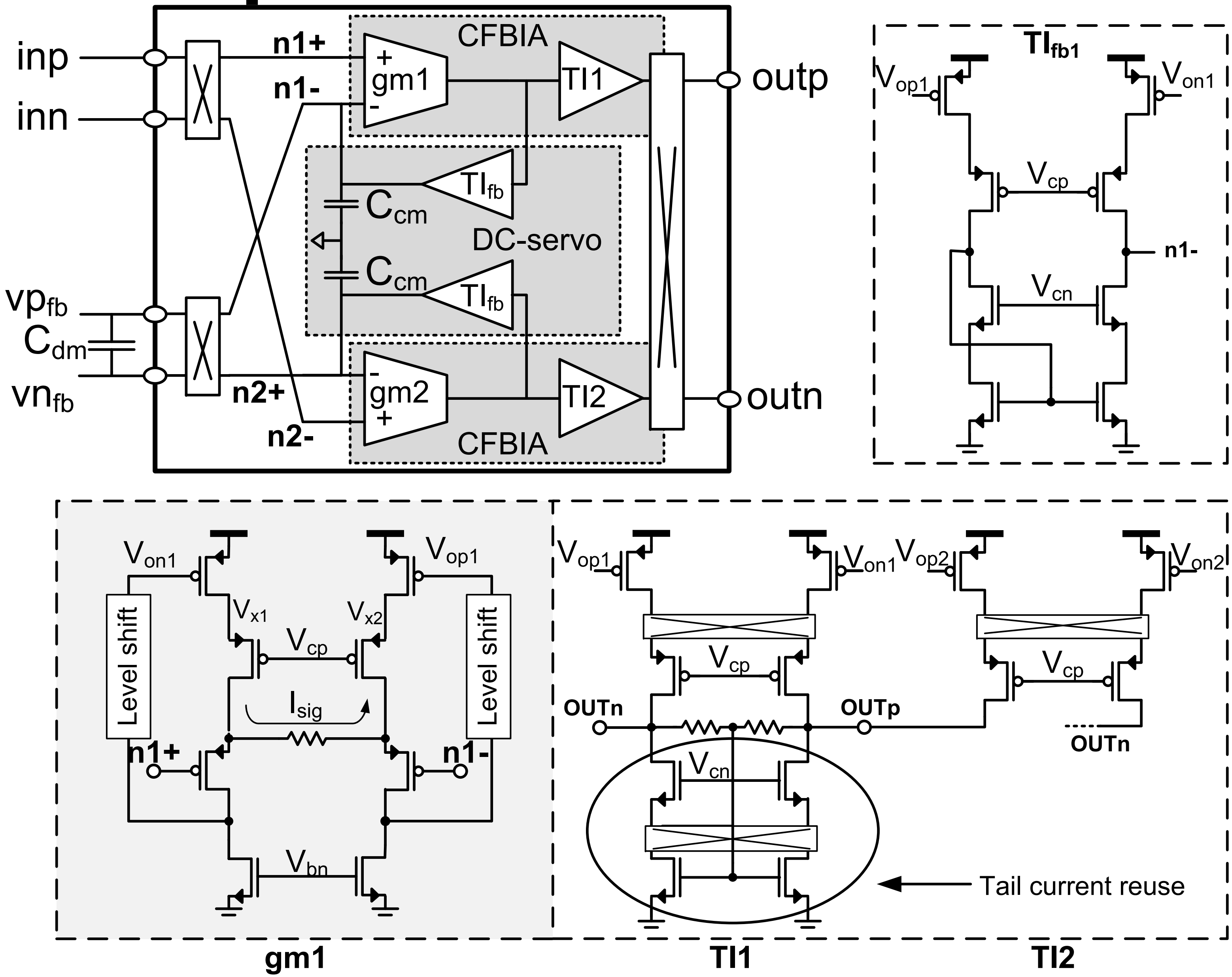
Proposed IA architecture



- Direct connection to body → High input impedance
- Pseudo differential IA (DDA alike input structure) → Can handle large offsets
- DC-offset subtracted at input → High gain possible
- DC-servo transparent for CM signals → High CMRR

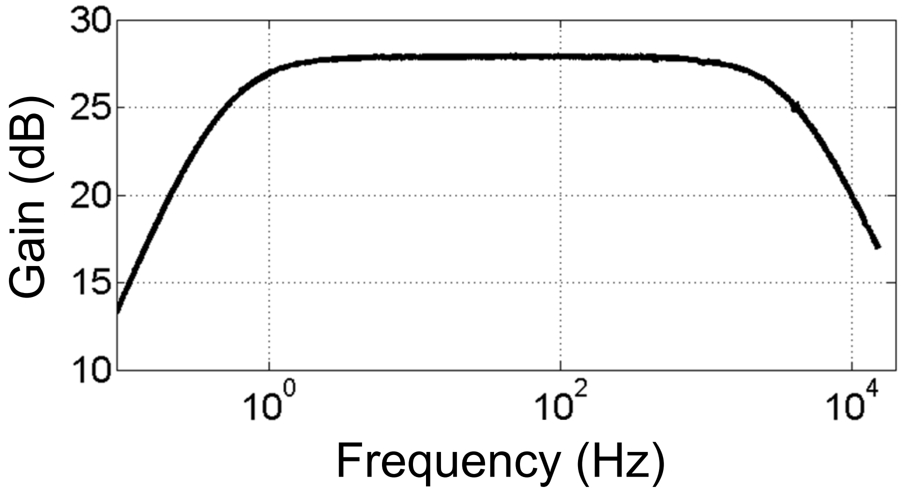
→ Only 1 ext. cap required

Proposed IA architecture

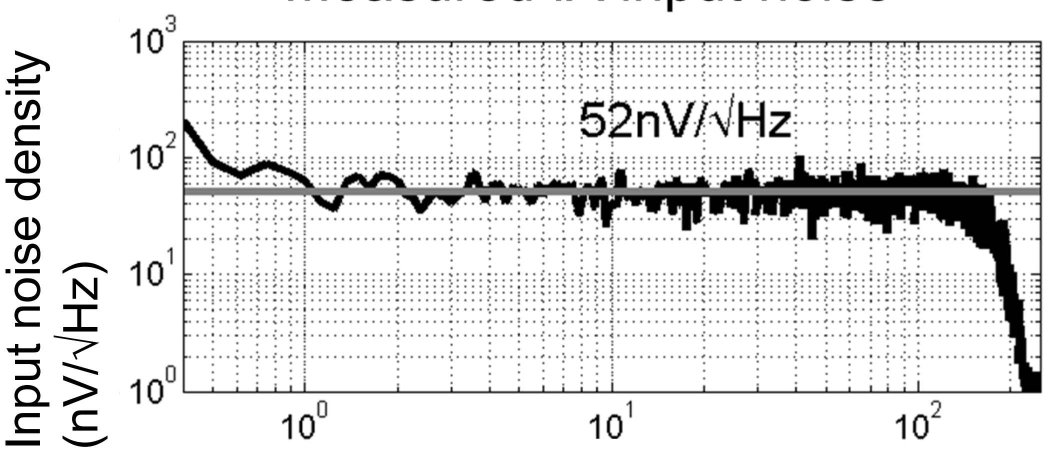


IA measurements

Measured IA transfer function



Measured IA input noise



Spec	Value
Tech.	0.18 μm
Power	16.5 μW
CMRR	> 110 dB
Input Imp. @50 Hz	> 500 MΩ
Input noise (100 Hz)	< 600 nVrms
Max. DEO	400 mV

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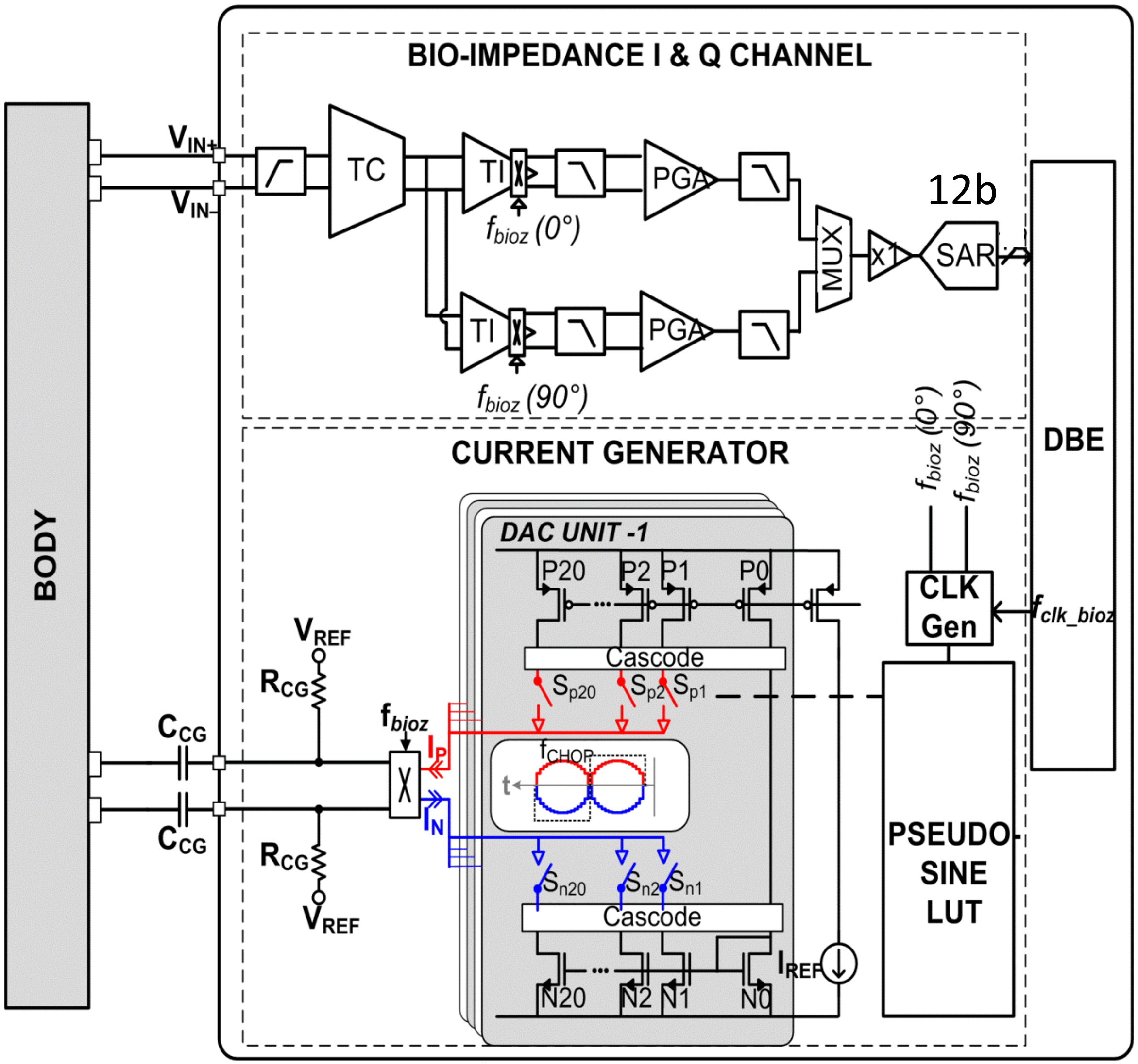
Bio-impedance architecture



[KIM – ISSCC 2013]

Channel readout

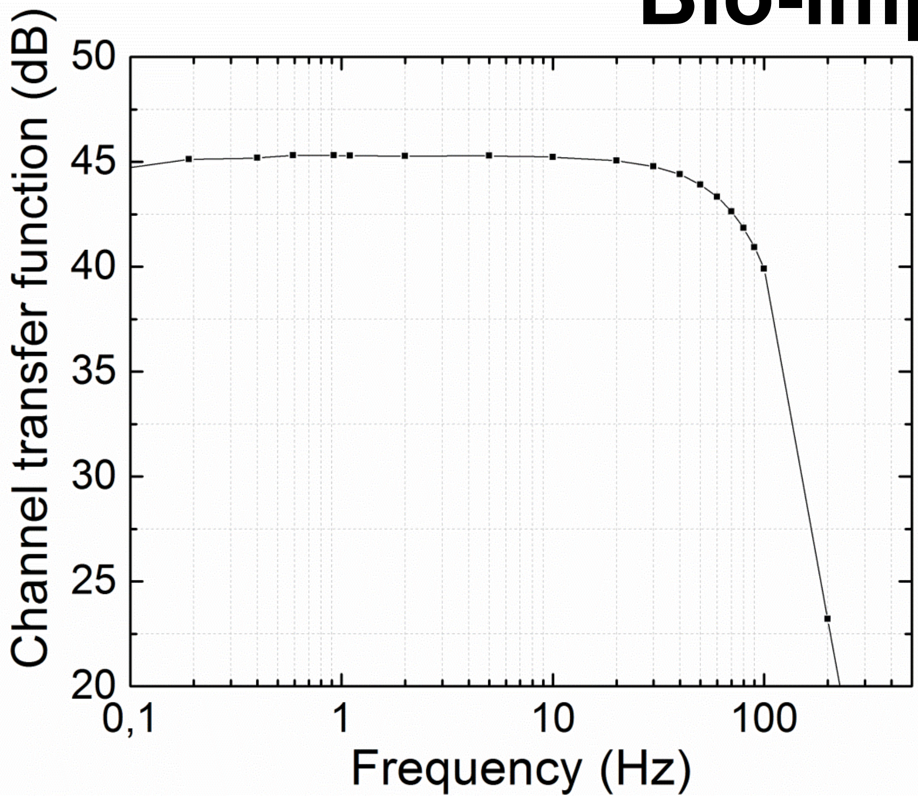
- I & Q components
- Low-noise, high performance IA
- Low-power

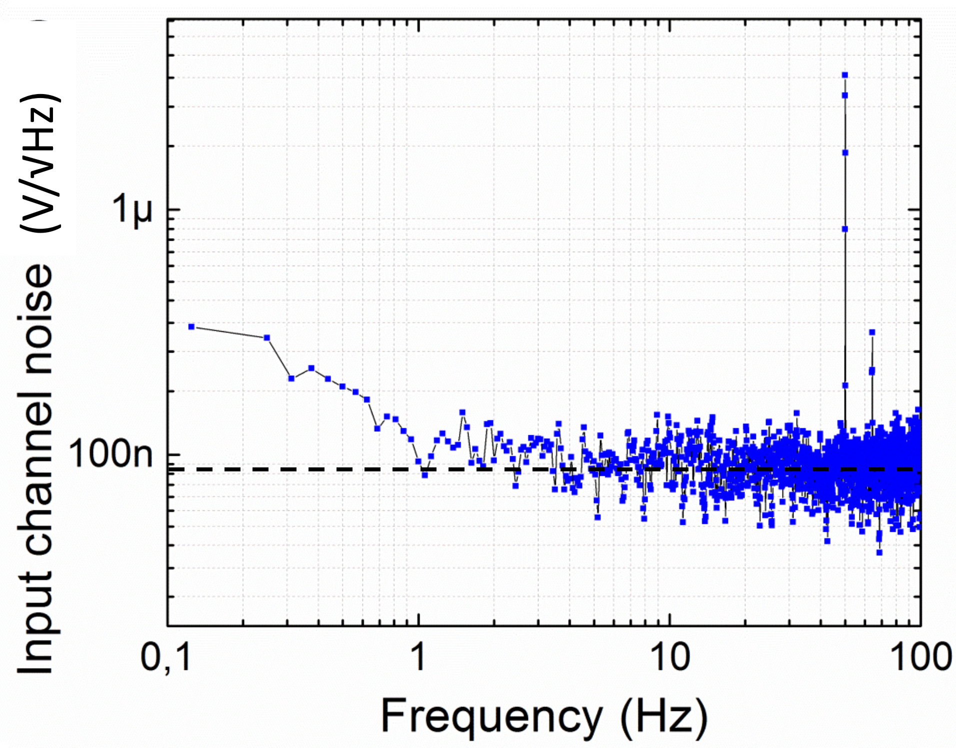
Current generator

- Fully integrated
- Support for square wave classic approach
- Dedicated pseudo-sine for low-power and high accuracy (low THD)

Measurement results

Bio-impedance





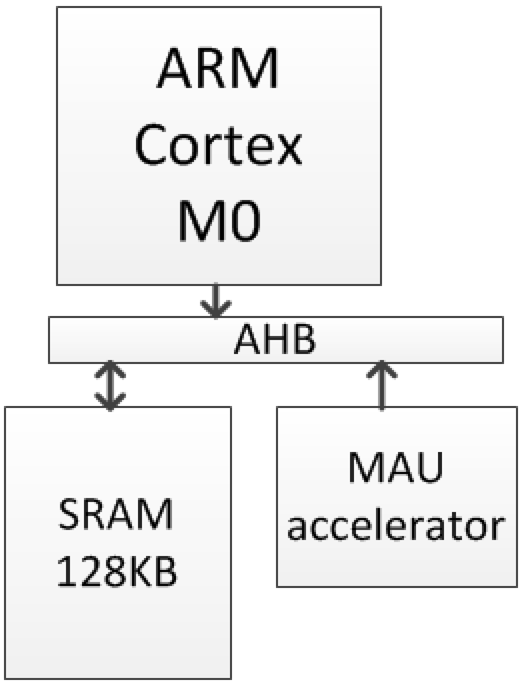
- Programmable gain 31-45dB
- Dynamic range 72dB
- Programmable current amplitude 9/18/27/36μApp @ 20kHz
- Power 58μW

Contents

Accelerator for V&M operations Motivation

- ARM Cortex M0 processor is popular for embedded applications
  - Ease of programming
  - Availability of tools and hardware
- However:
  - optimized for controlling tasks.
  - DSP tasks (like data filters) not well supported ➡ needs many more cycles
- Dedicated accelerators for DSP tasks to off-load Cortex M0
  - Less cycles to complete the tasks
  - Less power per cycle
  - Easy to use

Accelerator for V&M operations Functions



- Transposed multiplication

$$R_{nn} = A_{nm} \cdot A^{T}_{mn}$$

n = 1..4, m = 1 ... 5120

- Matrix multiplication

$$R_{qm} = B_{qn} \cdot A_{nm}$$

q,n = 1..4, m = 1 ... 5120

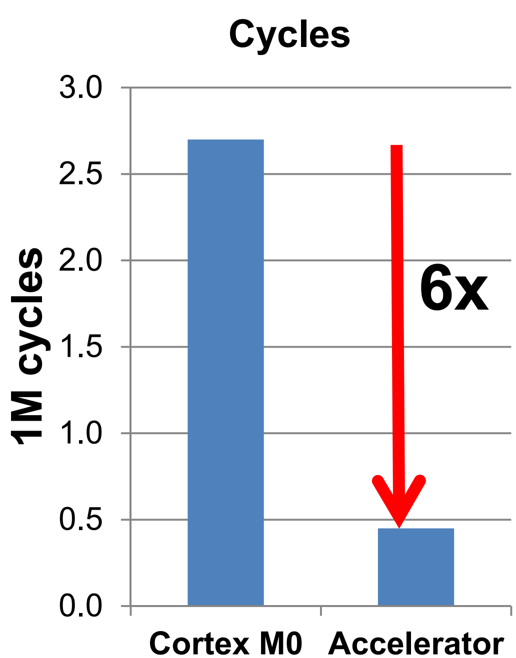
- Matrix row summation

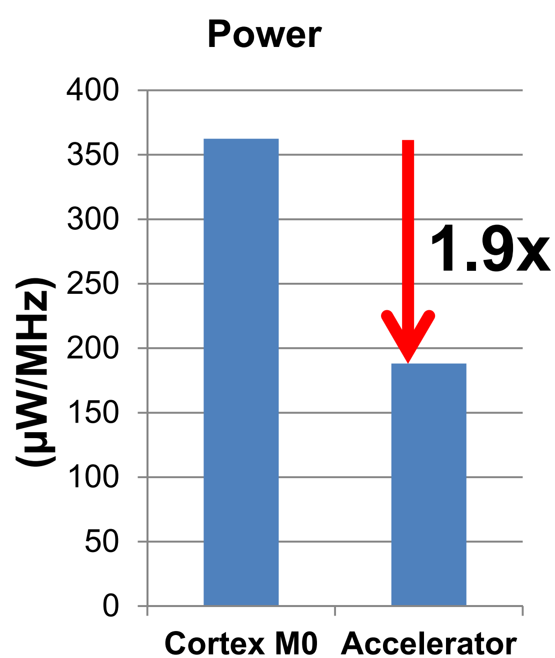
$$R_{m} = \sum A_{1m}, A_{2m}, A_{3m}, A_{4m}$$

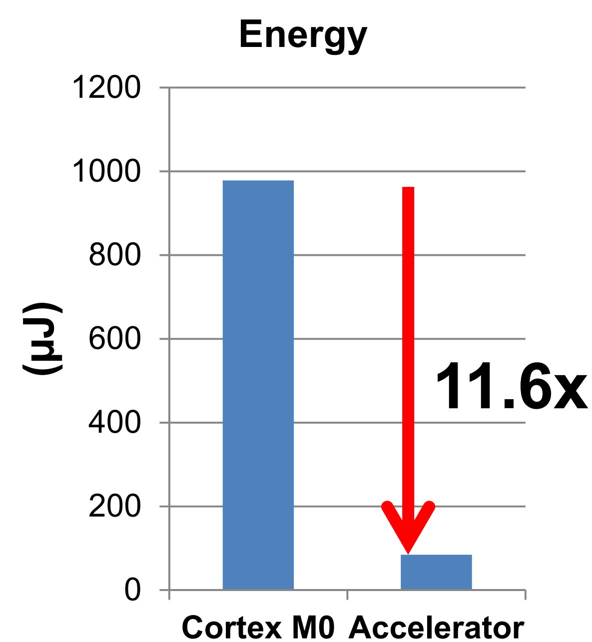
- ICA inner loop

Accelerator for V&M operations Measurement results

- Perform $A*A^T$ in DMA mode
- Both on Cortex M0 and on accelerator







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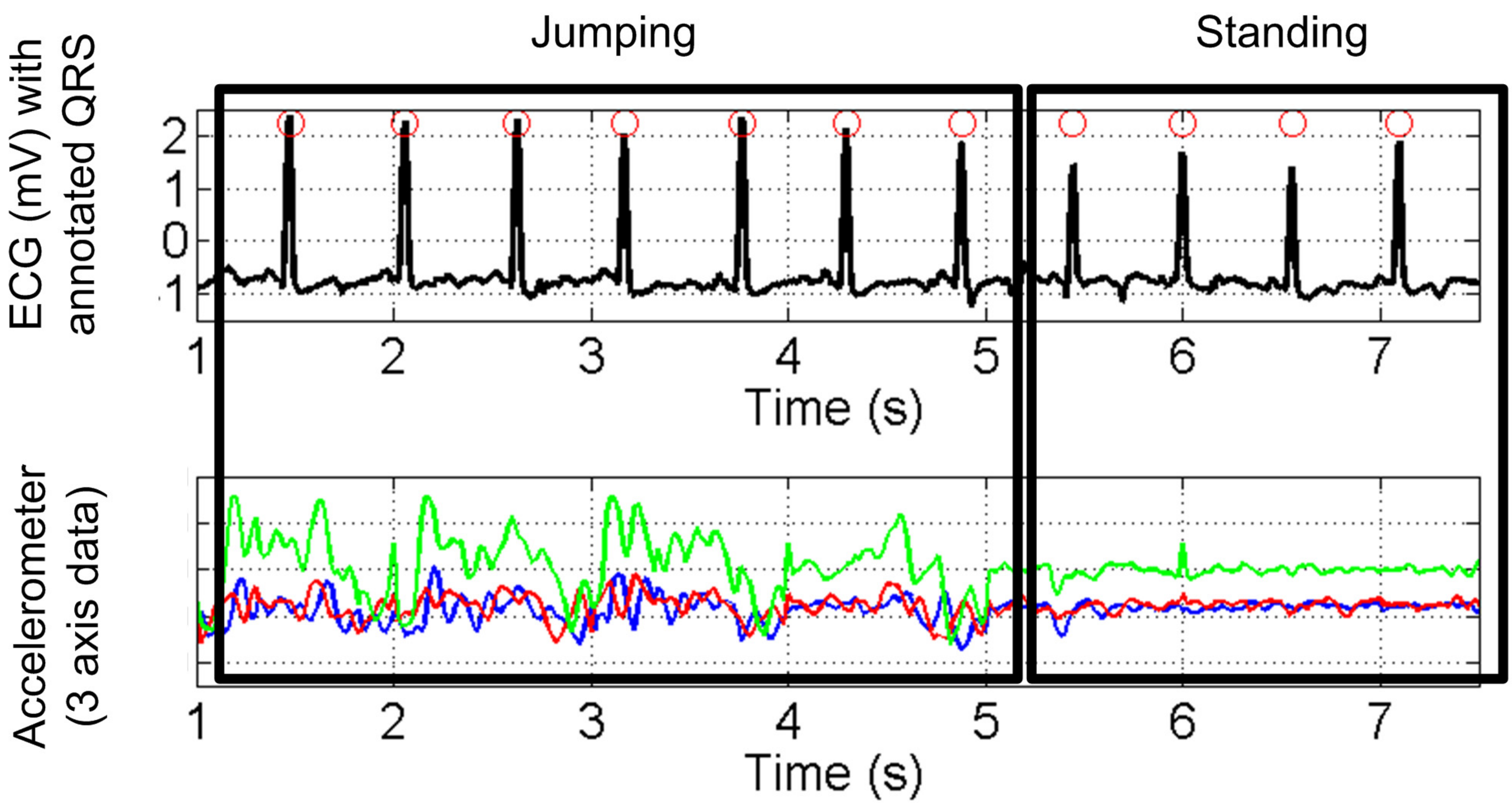
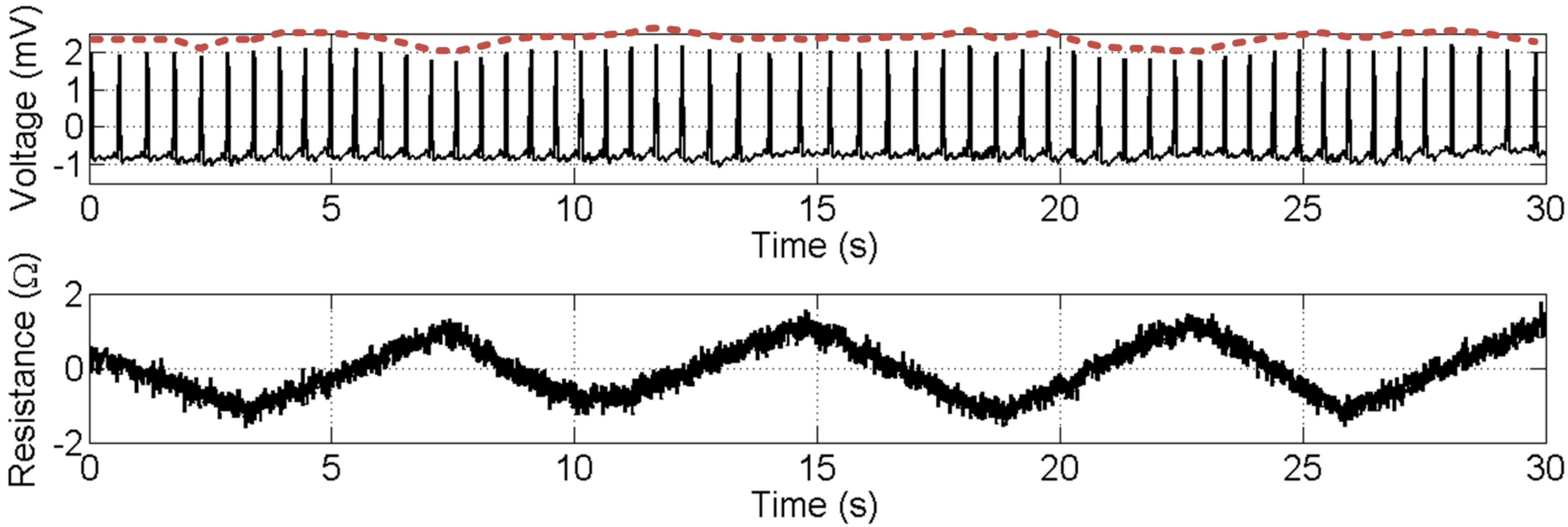
Measurement results



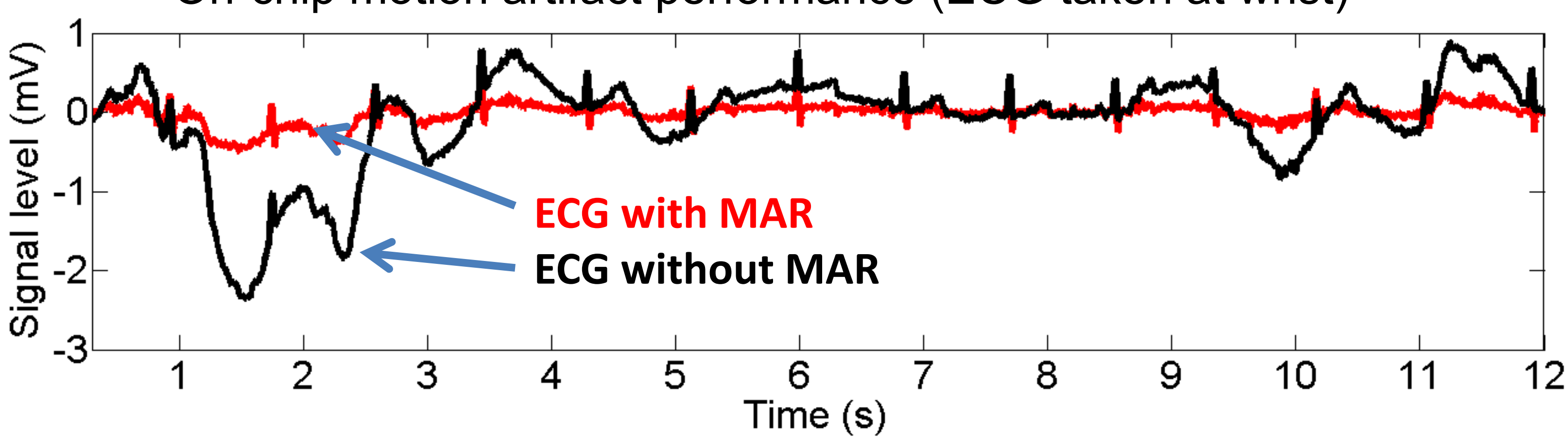
- ECG while jumping and standing
- On-chip QRS detection (CWT based)
- Concurrent 3-axis accelerometer data

Measurement results

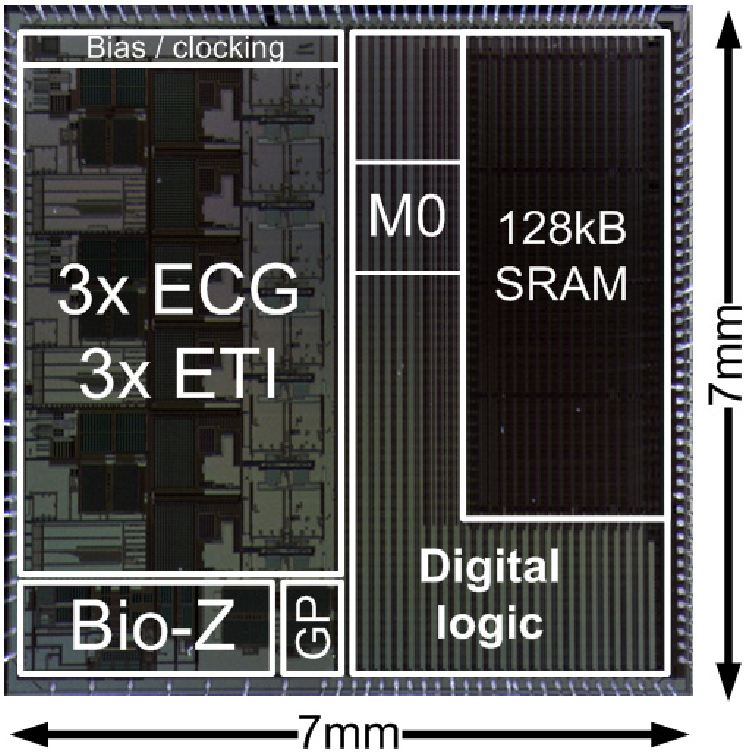
- ECG and concurrent respiration (bio-impedance)

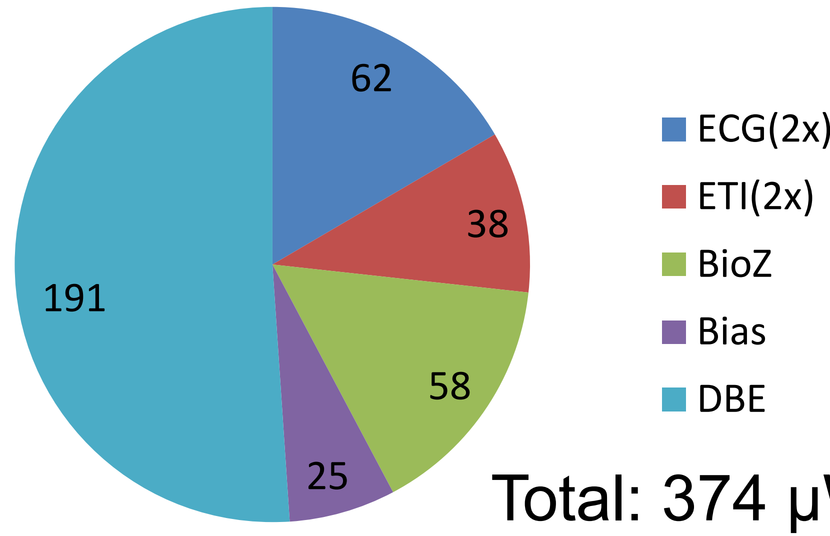


- On-chip motion artifact performance (ECG taken at wrist)



Performance measurements





Total: 374 µW

Power of commercial memories: 185 µW@1.8V

Application:

- Data collection from multiple sensors:

  2 ECG+ETI, Bio-impedance and accelerometer
- Executing: MAR and CWT-based R-peak detection

Features		This work	[Wong-08]	[Infineon]	[Kim-13]	[TI]
AFE	ECG	**√ (3)**	√ (1)	√	√ (3)	√
	Lead-off	√	-	-	-	√
	MAR	√	-	-	-	-
	Bio-impedance	√	-	-	√	√
	General purpose readout	**√ (2)**	√	√	-	-
DSP	Micro-processor	**Cortex M0**	8051	Cortex R4	-	-
	Accelerators	√	-	-	-	-
Technology (µm)		**0.18**	0.13	n.a.	0.18	n.a
Supply Voltage (V)		**1.2 (1.8)**	1	3.3	1.8	3

Performance		This work	[Wong-08]	[Infineon]	[Kim-13]	[TI]
Bio-potential readout	Input Noise (0.5-150Hz)	**605nVrms**	n.a.	n.a.	2000nVrms	900nVrms
	CMRR	**>110dB**	n.a.	n.a.	100	>105dB
	Diff. input range	**±400mV (DC) 30mVpp (AC)**	n.a.	540mVpp	60mVpp	600mVpp
	ADC	13.5b SD-ADC	10b SD-ADC	16b SD-ADC	9.3b SAR	17.14b SD-ADC
	Power ECG/channel	31 μW 56 (incl. bias)	10 μW	n.a.	0.82 μW	335 μW
	Power ECG+ETI/ch	50 μW 75 (incl. bias)	n.a.	n.a.	n.a.	n.a.
Bio-impedance readout	Resolution	**8.6 mΩ /√Hz @ 36 μApp, 20kHz pseudo-sine**	n.a.	n.a.	8.8 mΩ /√Hz @ 40 μApp, 20kHz pseudo-sine	4.7 mΩ/√Hz @ 30 μApp, 32kHz square
	Power	58 μW (incl. CG, ADC)	n.a.	n.a.	56.2 μW	335 μW (excl. CG)
Digital	Processor clock	1-20 MHz	32k or 16MHz	96MHz	n.a.	n.a.
	On-chip memory	128 KB	64KB	384 KB	n.a.	n.a.
	Power (sleep)	<10 μW	5 μW	~30 μW	n.a.	n.a.
	Power (active)	**120 μW/MHz**	500 μW/MHz		n.a.	n.a.

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Summary

- A SoC has been developed with
  - Multi-sensor support including high performance AFE having 3-lead ECG+ETI (50 μW) and bio-impedance (58 μW) readouts
  - High performance IA in terms of noise (<600 nVrms) , input impedance (>500 MΩ) and CMRR (> 110 dB)
  - Generic low-power DBE consisting of ARM Cortex M0, HW MAR, matrix multiply-accumulate accelerator (saves more than factor 11 in energy)
  - Low power: 374 μW for 2Ch. ECG, BioZ, accelero, with (HW) MAR and CWT R-peak detection

- Key enabler for numerous emerging personal health applications

A 4.9mΩ-Sensitivity Mobile Electrical Impedance Tomography IC for Early Breast-Cancer Detection System

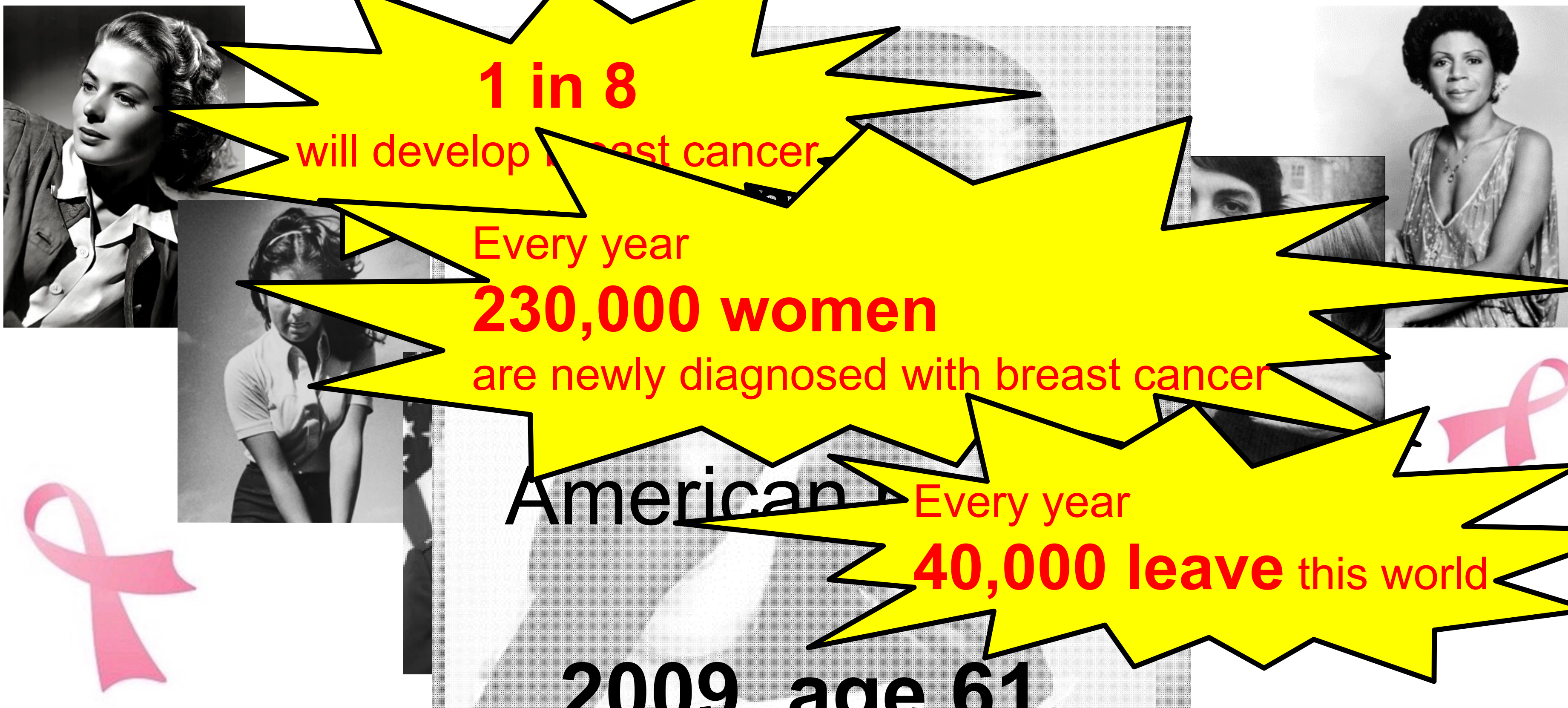
Sunjoo Hong, Kwonjoon Lee, Unsoo Ha,
Hyunki Kim, Yongsu Lee, Youchang Kim
and Hoi-Jun Yoo

Semiconductor System Laboratory
Dept. of EE, KAIST

Outline

- Motivation
- EIT Breast Cancer Detection System
- Electrical Impedance Tomography (EIT) IC
  1. Low-distortion Current Stimulator
  2. High-sensitivity Voltage Sensor
- Implementation Results
- Conclusion

Motivation



1 in 8
will develop breast cancer

Every year
230,000 women
are newly diagnosed with breast cancer

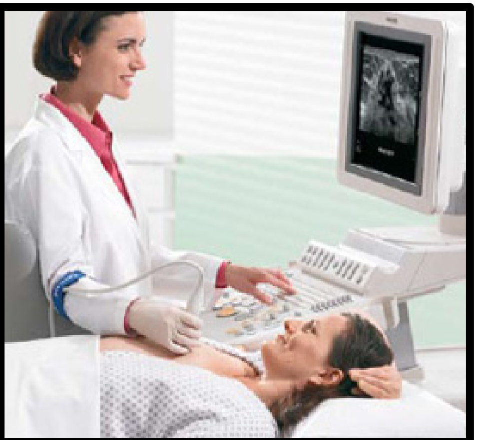
Every year
40,000 leave this world

Early Detection & Treatment
→ Reduce breast cancer mortality by 30%

* http://www.breastcancer.org, 2013.

Breast Cancer Detection (BCD)

- In hospital,



X-ray Mammography | Ultrasound

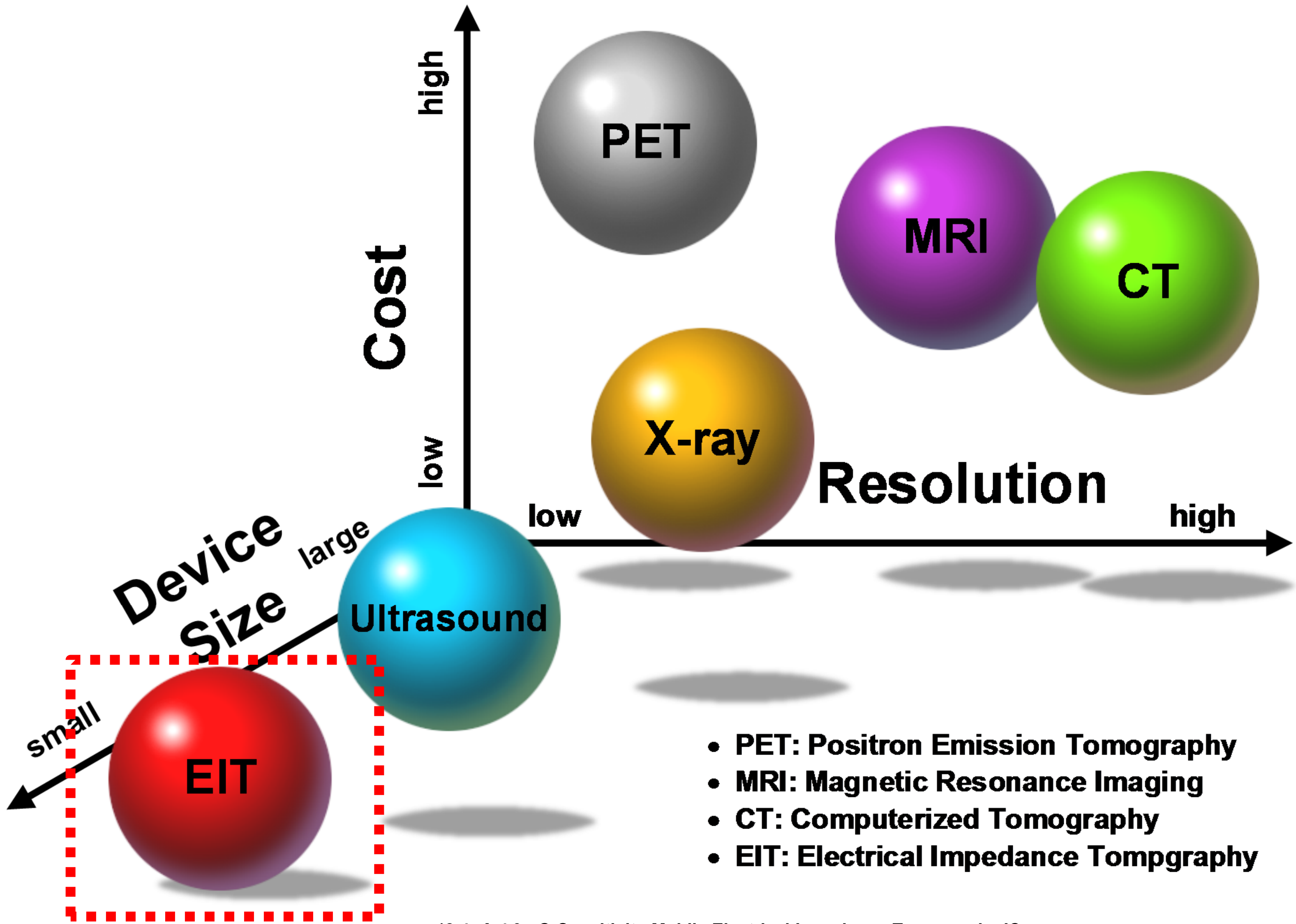
☺ High resolution
☹ Radiation & expensive
☹ Pressure

- At home,

Palpation

☺ Easy & simple
☹ Poor detection ratio

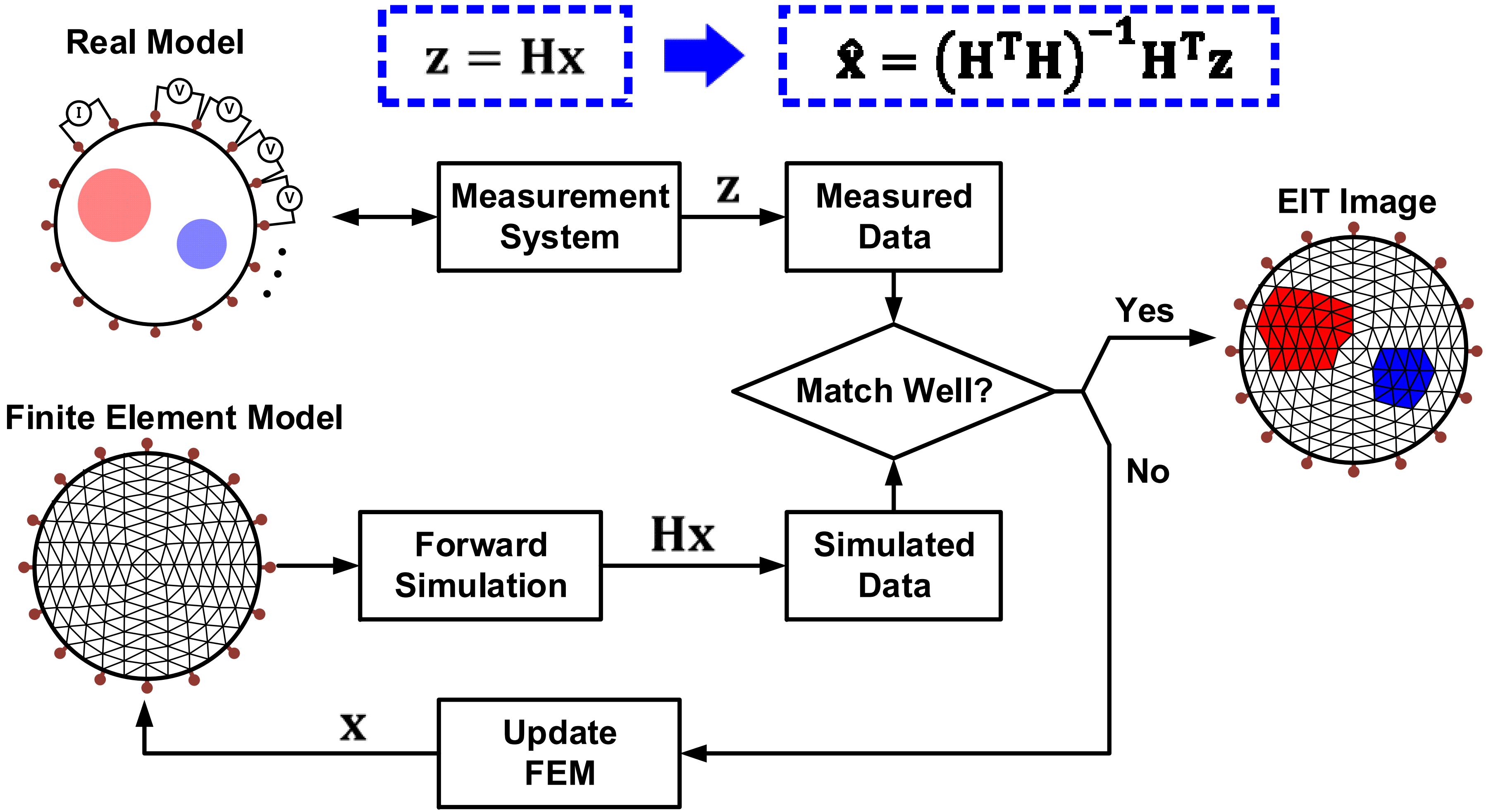
Breast Imaging Methods



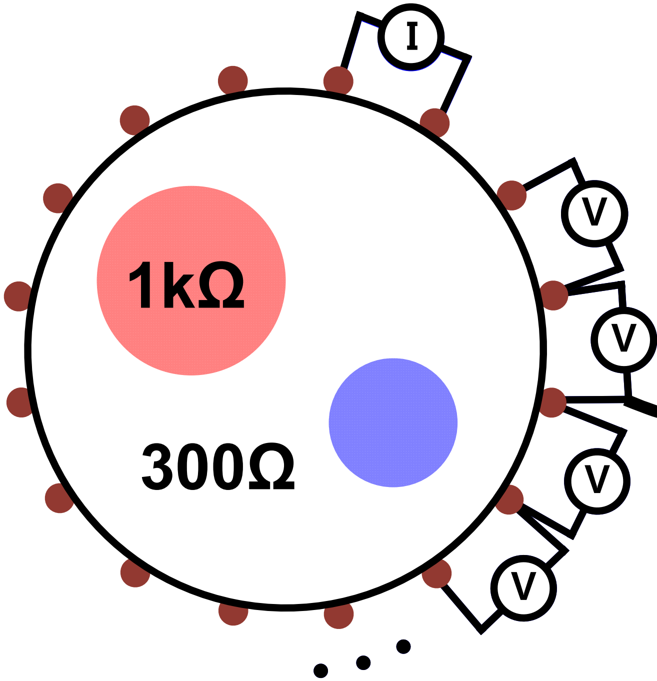
- PET: Positron Emission Tomography
- MRI: Magnetic Resonance Imaging
- CT: Computerized Tomography
- EIT: Electrical Impedance Tompgraphy

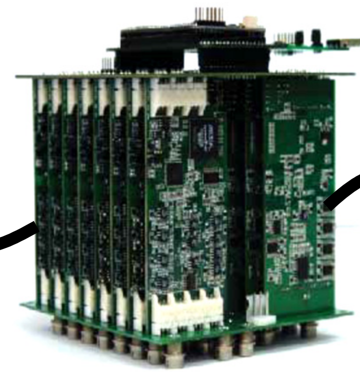
Principles of EIT

- Electrical Impedance Tomography (EIT)



Structure of EIT System

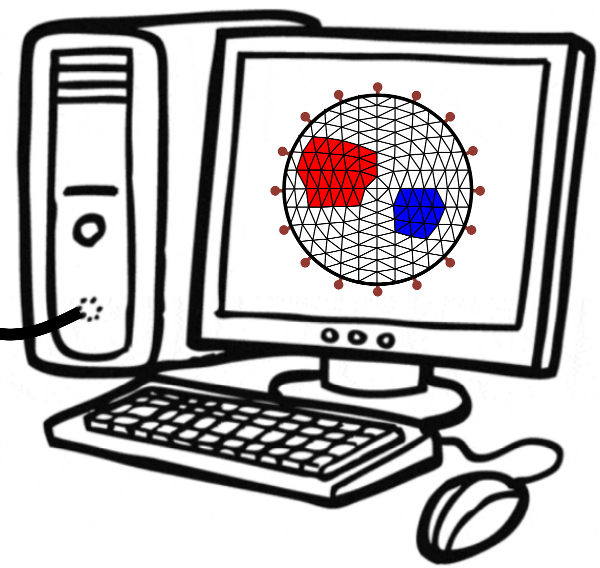




Current Source

Voltage Meter

Multiplexer

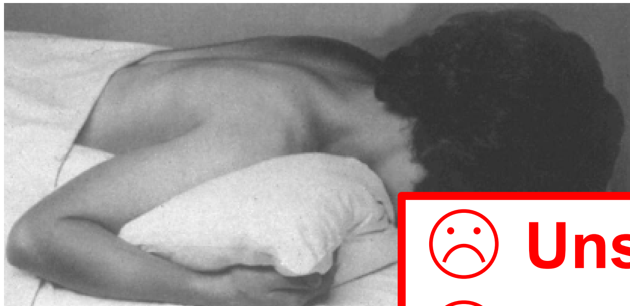


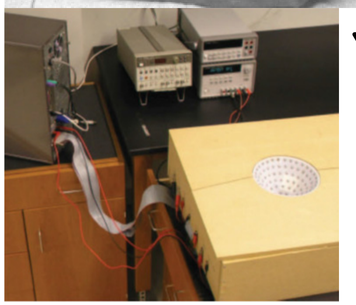
Electrode Array

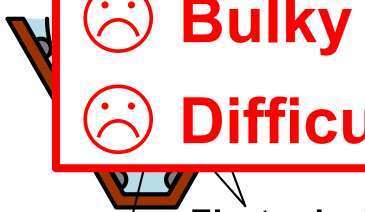
Imaging Device

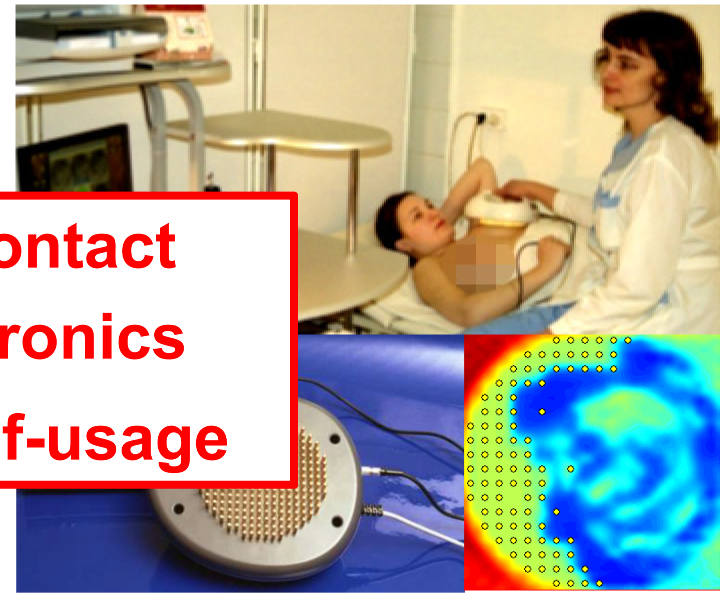
Stable Electrode Contact	Compact Measurement Device	Mobile Imaging

Previous EIT BCD System









- ☹ Unstable Contact
- ☹ Bulky Electronics
- ☹ Difficult Self-usage

Bed Type [1]

- Electrodes on the bucket
- Breast in liquid electrolyte
- Current diffusion

Probe Plate Type [2]

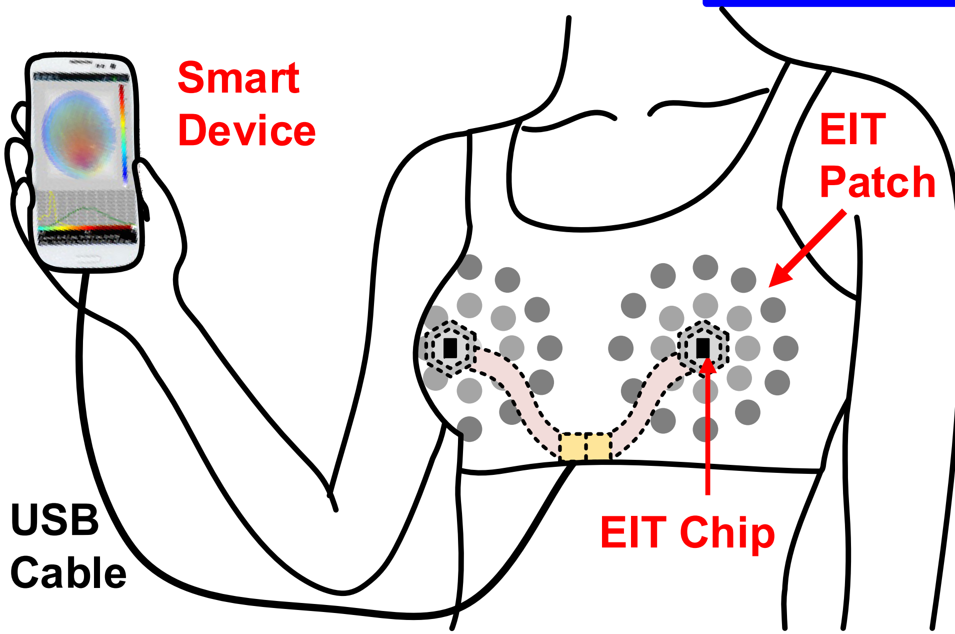
- Array of metallic rods
- Effective # of electrodes ∝ pressure
- 2D feature map

[1] Duke University, Microwave and Optical Technology Letters, 2008.
[2] Russian Academy of Sciences, Biomedical Engineering, 2012.

Proposed Early BCD System

- **Brassiere-type BCD System**
  - Soft electrodes on P-FCB*
  - Fully integrated IC for EIT
  - Imaging with smart device

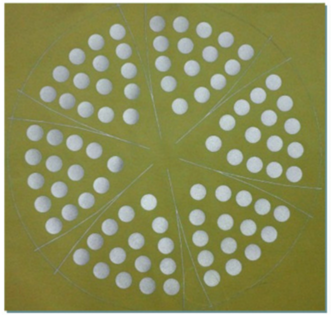
Stable Contact
Small Form Factor
Easy to Use



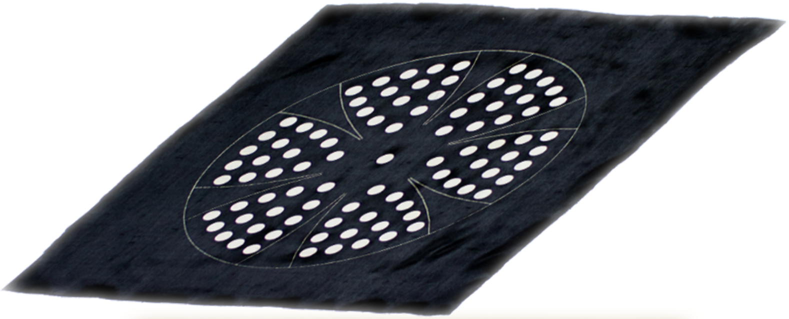
* Planar-Fashionable Circuit Board, ISSCC'08

P-FCB Electrodes

- Electrode on Fabric
  - Silver or Ag/AgCl paste screen printing
  - 2kΩ at 1kHz with 8mm diameter

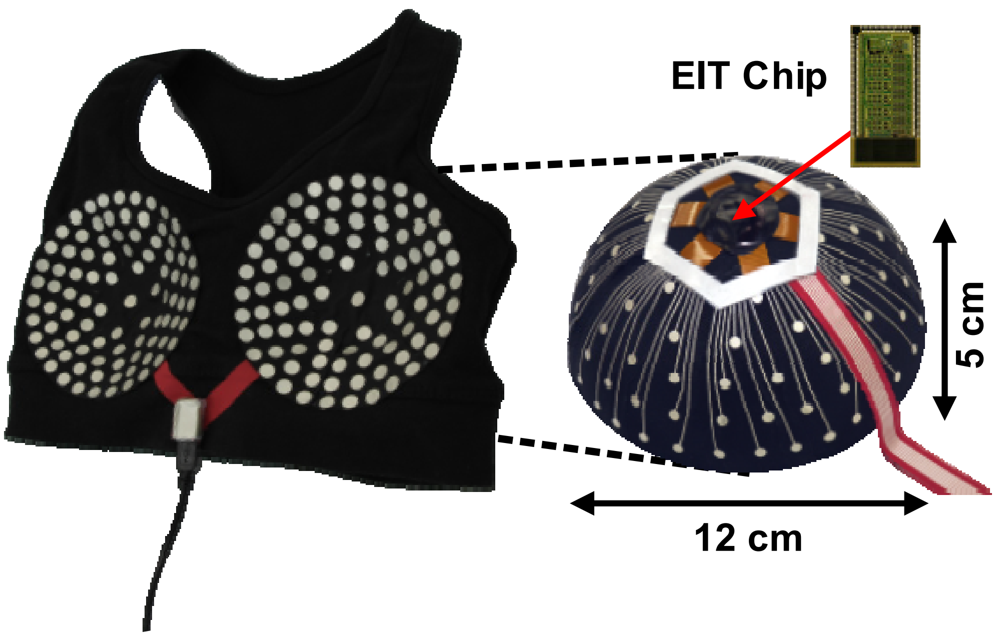


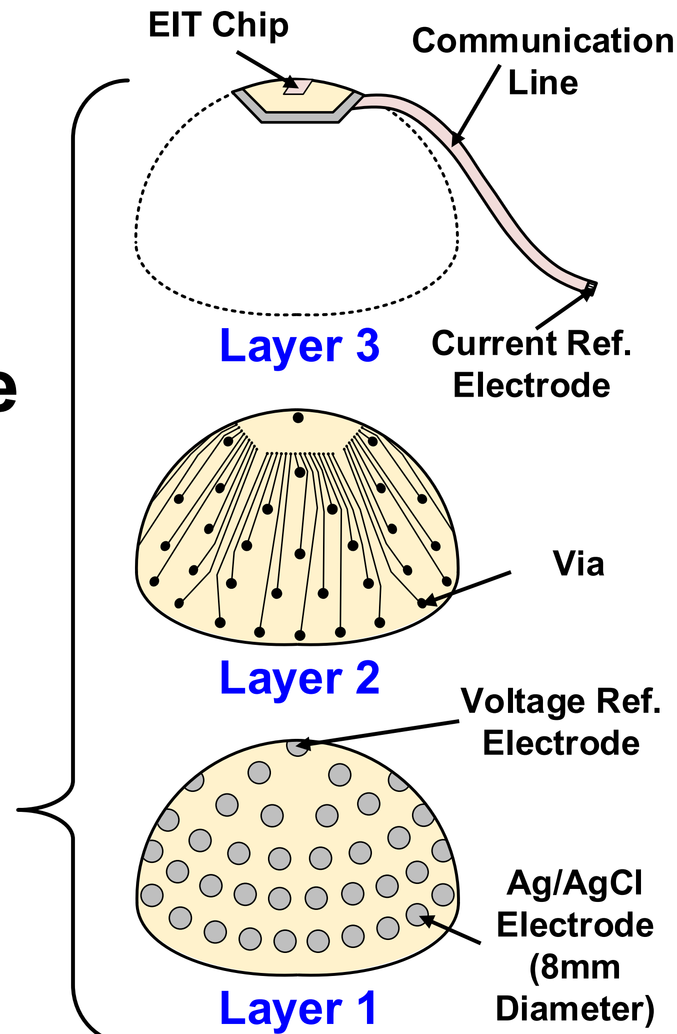
- Flexible and stable contact on the skin



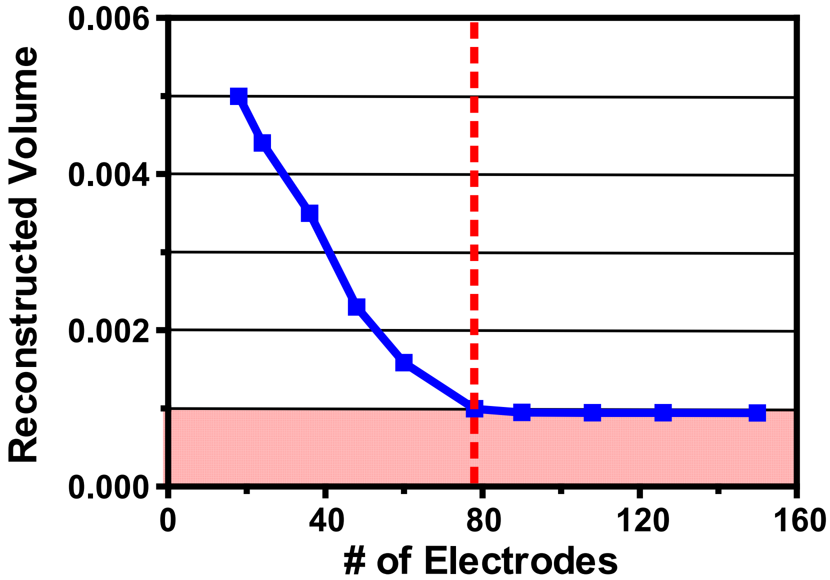
Wearable EIT Patch

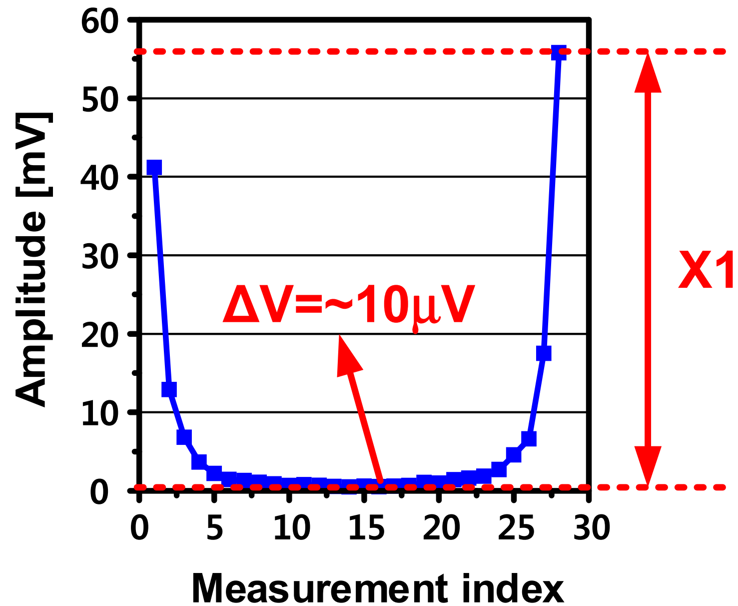
- ❑ **Layer 1:** Electrode array
- ❑ **Layer 2:** Electrode connection
- ❑ **Layer 3:** EIT chip & communication line





Design Requirements





- < 0.1% volume detection ➔ # of electrodes > 80
- < 1 min. scanning ➔ # of voltage channel > 5
- Large input variation
  : V_{min}=0.5mV±10μV, V_{max}=~100V_{min}
  ➔ voltage gain > 46dB & < 20dB

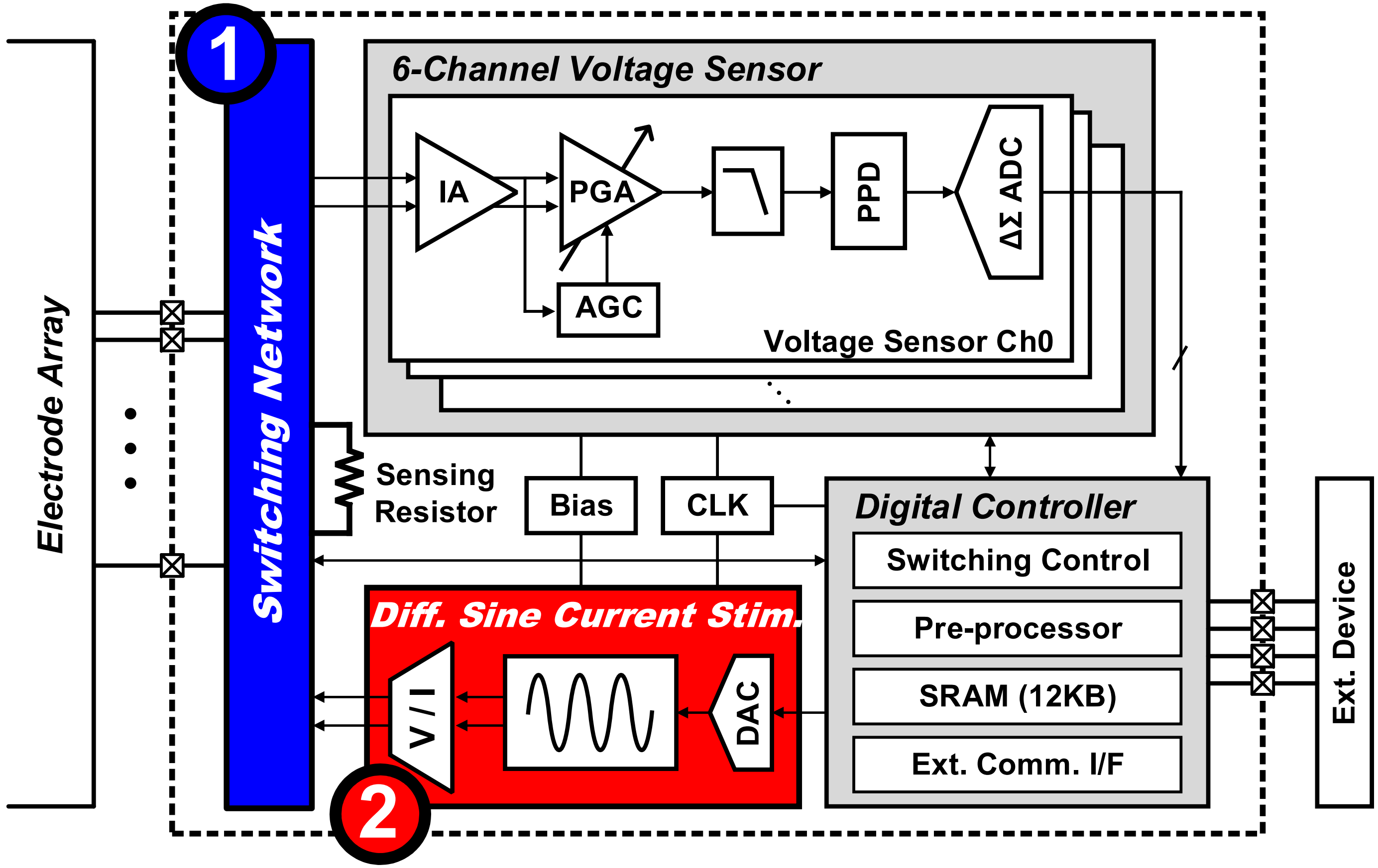
Key Features of the EIT IC

- ❑ **Low-distortion Current Stimulator**
  - – Differential Sine-Current Stimulator (DSCS)
    - ➔ Low distortion & programmability

- ❑ **High-sensitivity Voltage Sensor**
  - – Adaptive Gain Controller (AGC)
    - ➔ Large input dynamic range
  - – Peak-to-Peak Detector (PPD)
    - ➔ Lighten a burden imposed on the ADC and digital controller

EIT IC Architecture

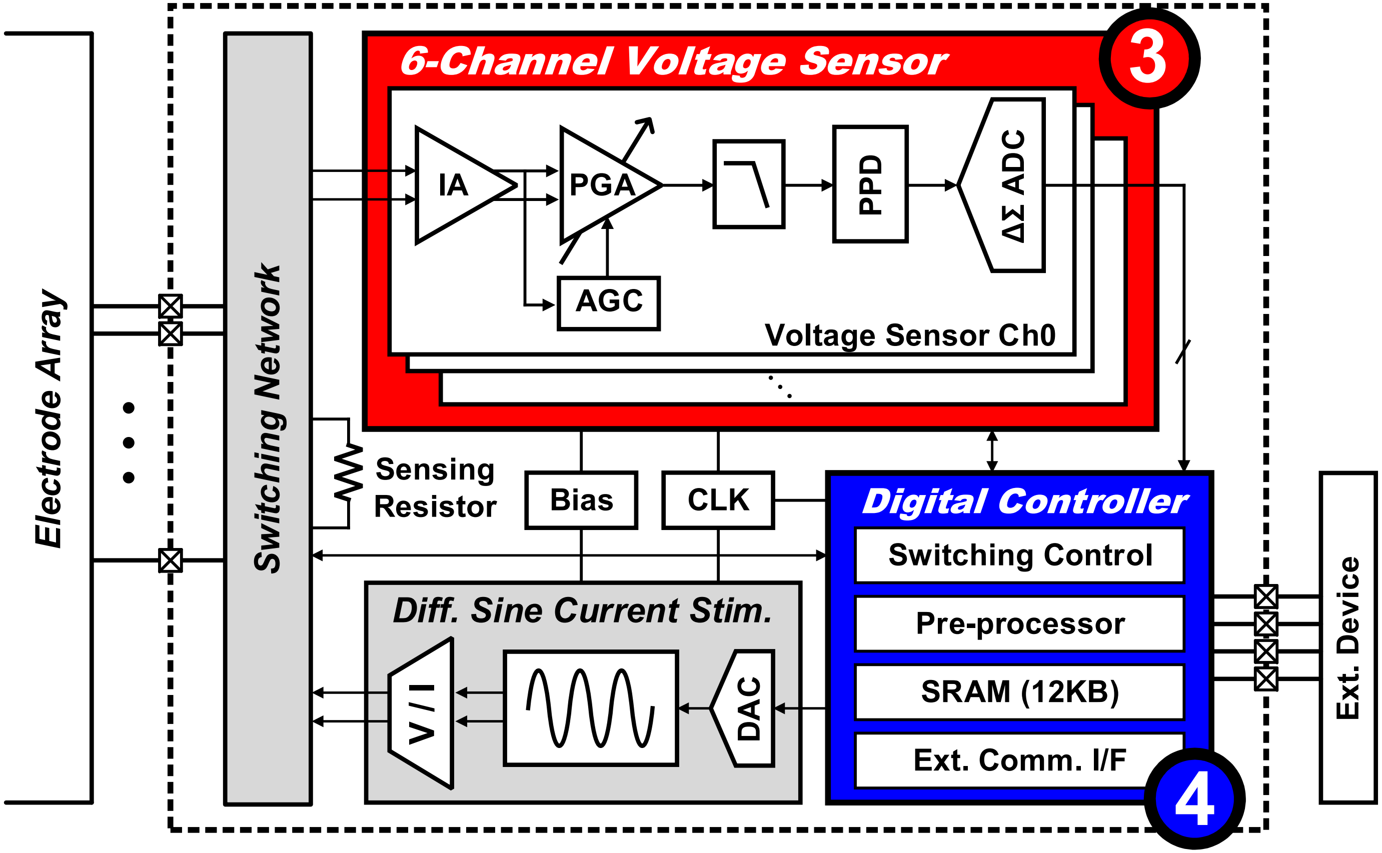
1. Switching Network → Reconfigurable measurement modes
2. DSCS → Low distortion programmable current stimulation



EIT IC Architecture

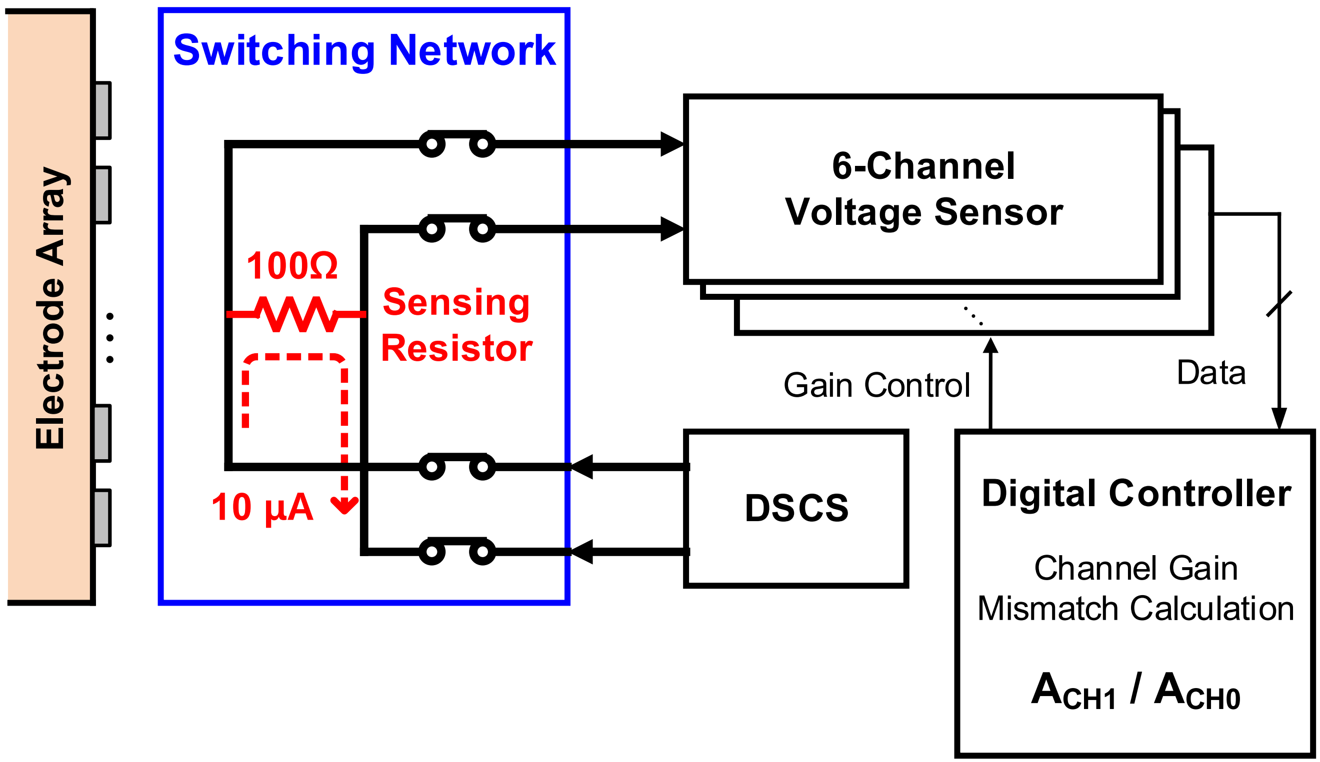
3. 6-Channel Voltage Sensor ➔ High-sensitivity sensing

4. Digital Controller ➔ System control and data calibration



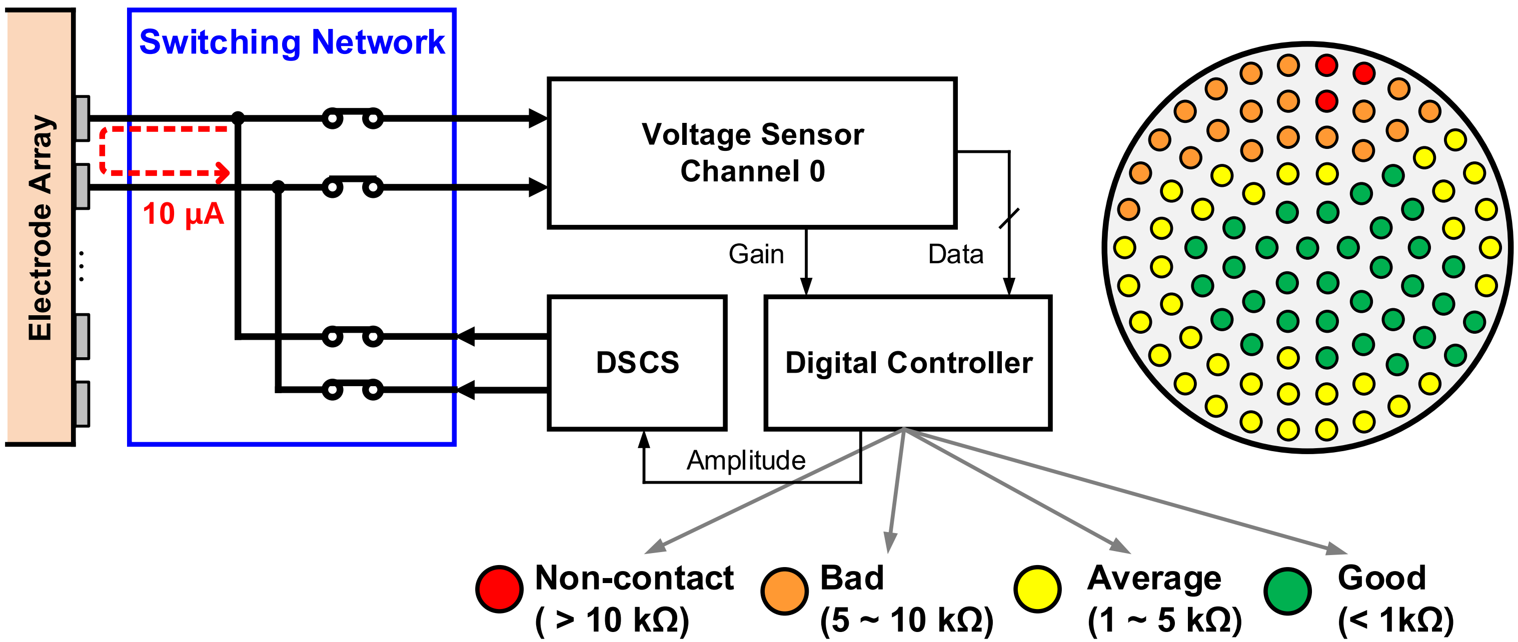
3 Modes of Operation - GS

- ❑ **Gain Scanning (GS) Mode**
  - – Gather gain mismatch information of 6-channel voltage sensor



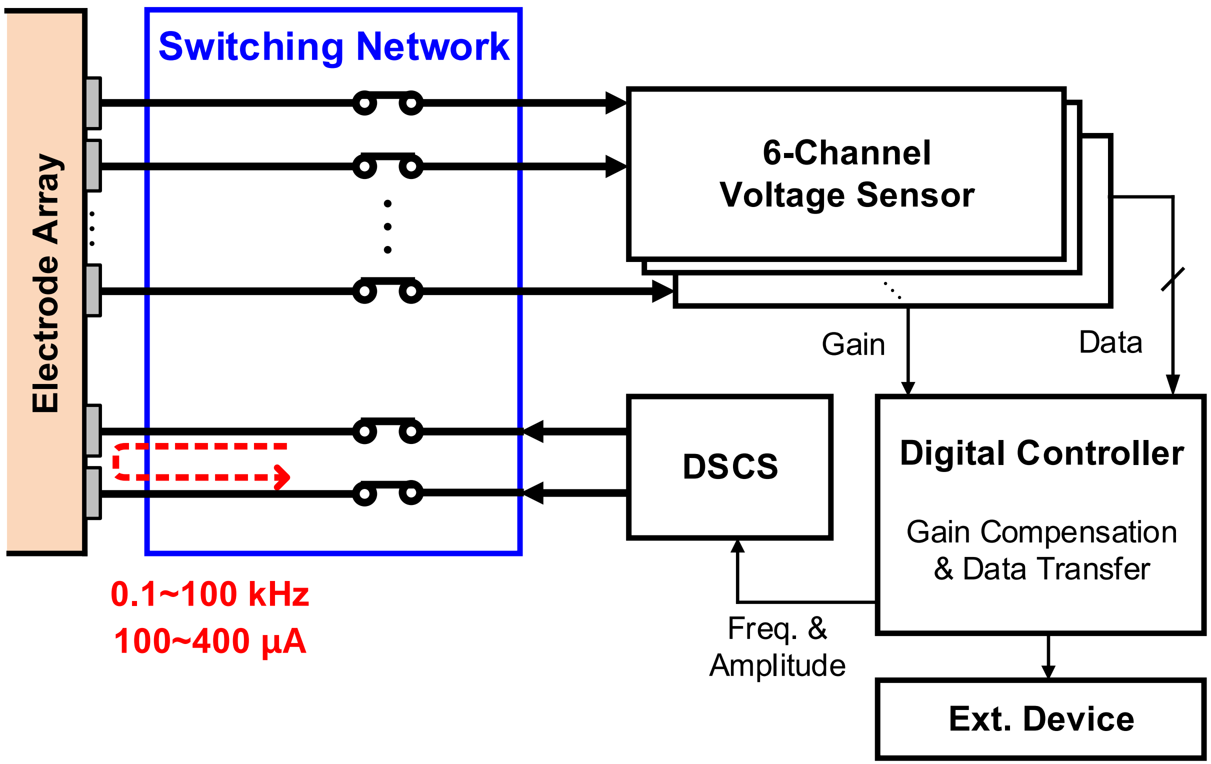
3 Modes of Operation - CIM

- Contact Impedance Monitoring (CIM) Mode
  - Make **reliable contact** (<1kΩ, 1st manually calibration)
  - Determine amplitude of stimulation current
  - 2nd calibration in imaging



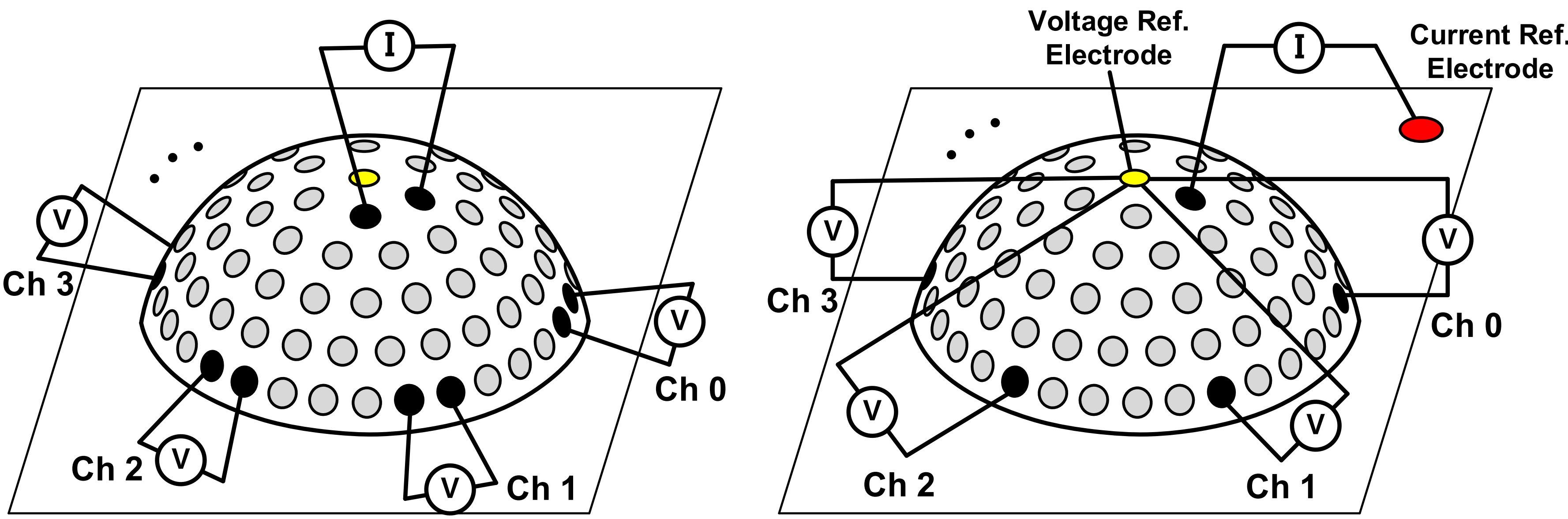
3 Modes of Operation - EIT

- ❑ Electrical Impedance Tomography (EIT) Mode
  - – **Reconfigurable switching** for various imaging algorithm



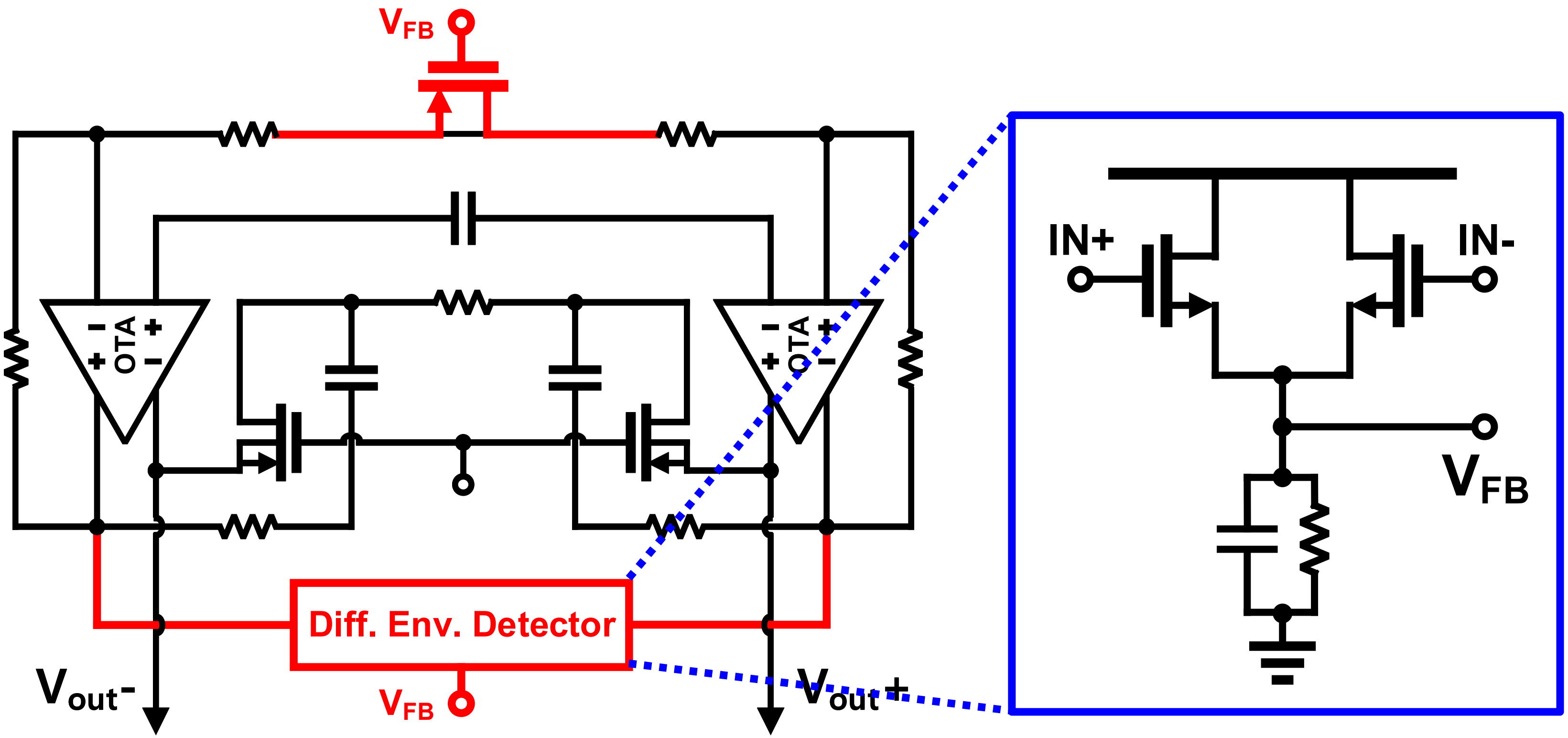
3 Modes of Operation - EIT

- Electrical Impedance Tomography (EIT) Mode
  - Reconfigurable switching for various imaging algorithm



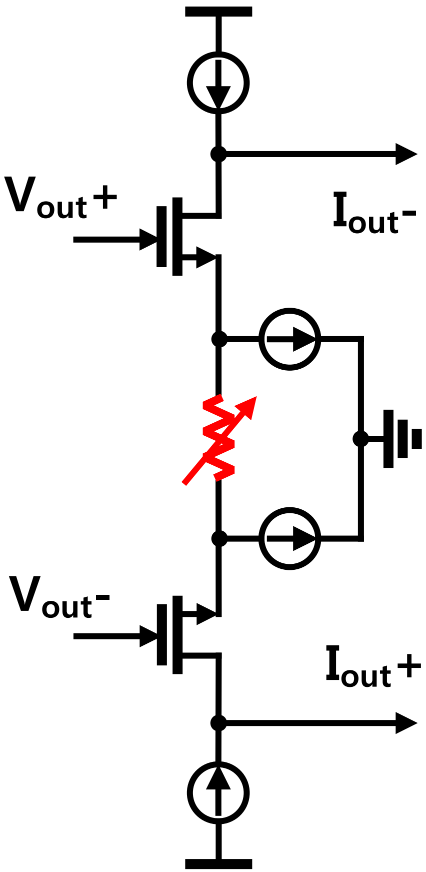
Diff. Sine Current Stimulator (DSCS)

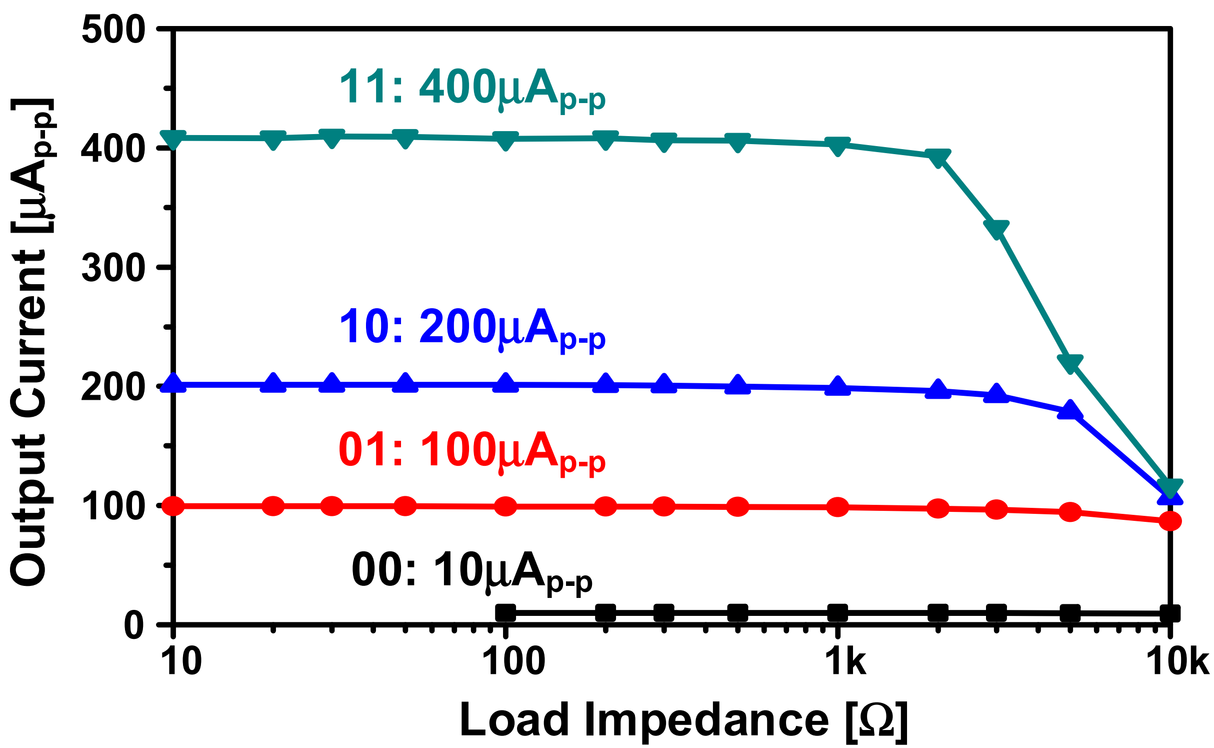
- **Fully Diff. Sine Voltage Generator**
  - Balanced structure ➔ 2nd harmonic reduction
  - Loop gain adjustment ➔ further harmonic reduction



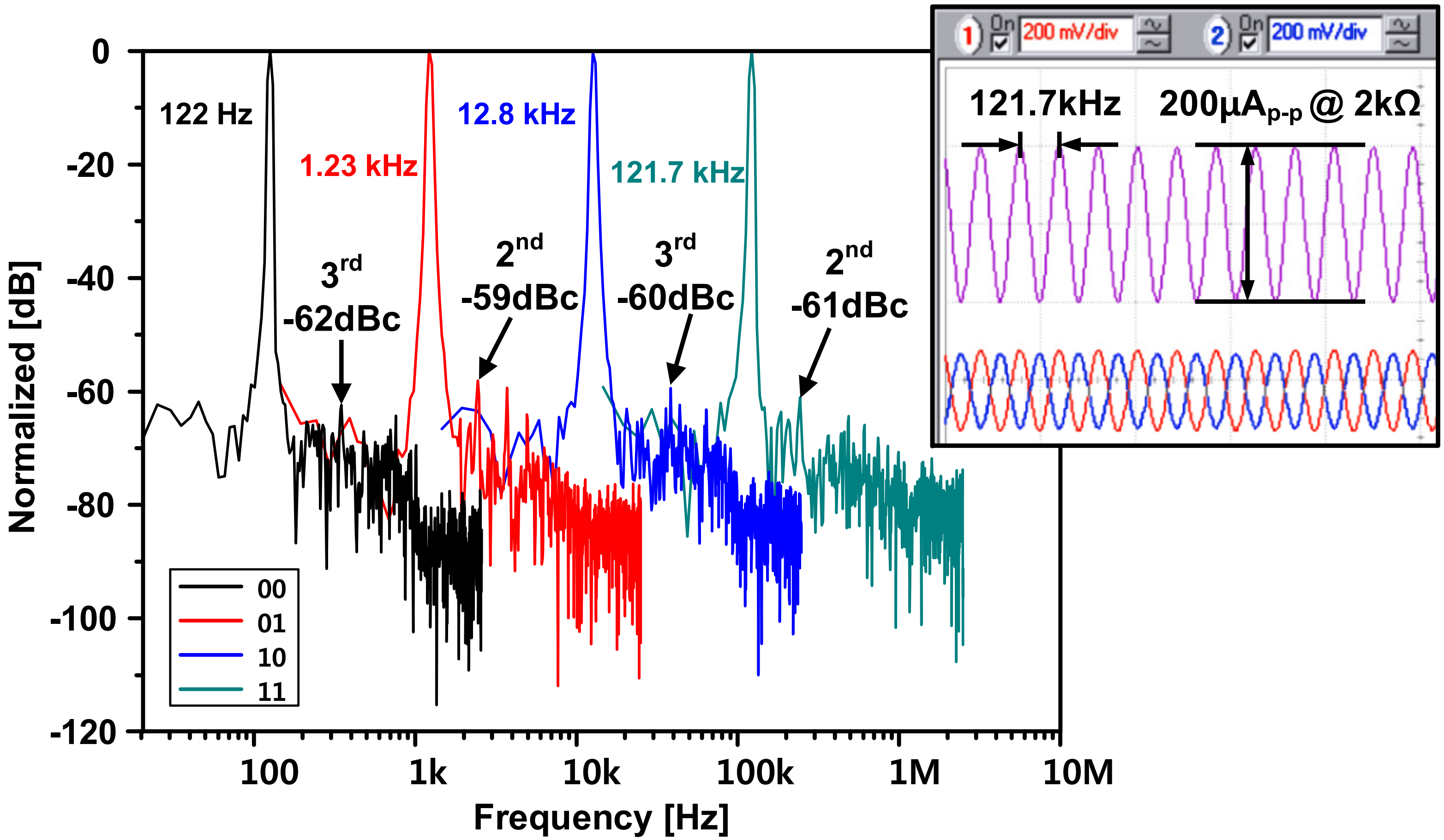
Diff. Sine Current Stimulator (DSCS)

- V/I Converter
  - Amplitude control ➔ 10 - 400 μA_{p-p}





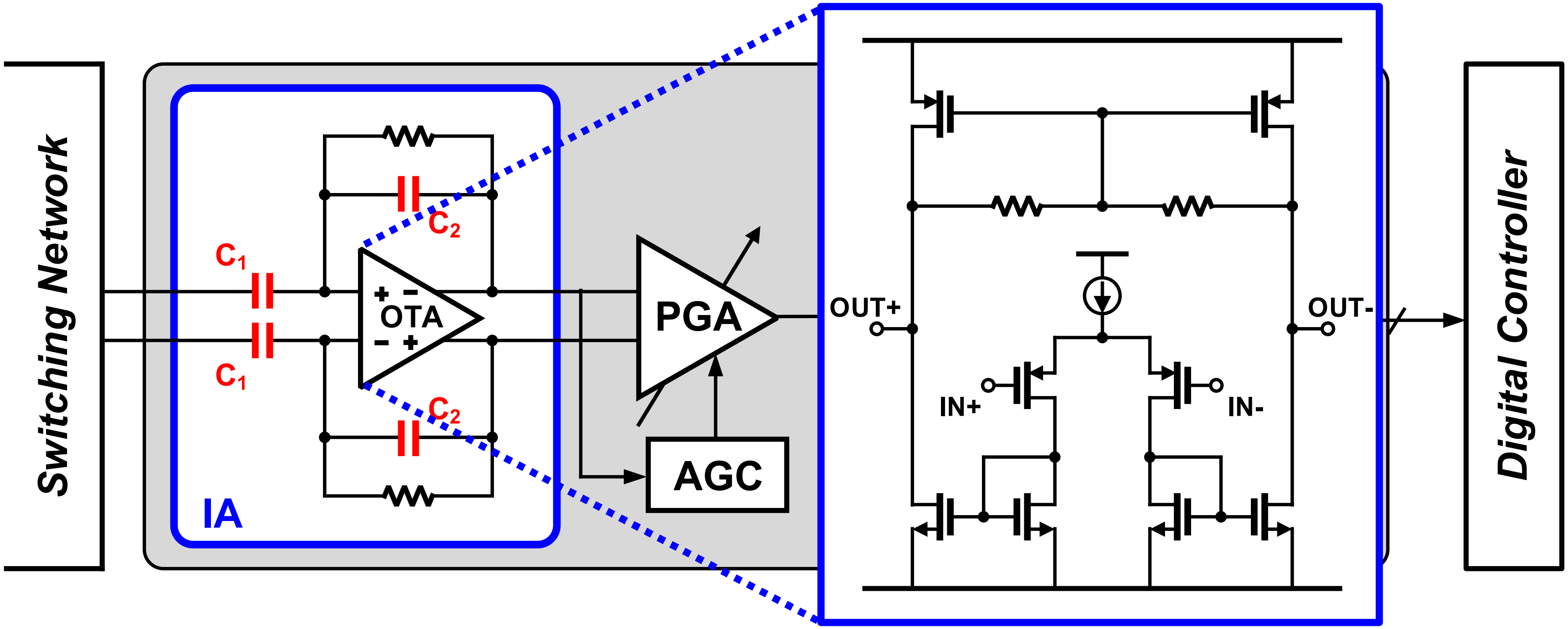
Measurement of DSCS



➔ Variable frequency w/ < -59dBc @ 2kΩ Load

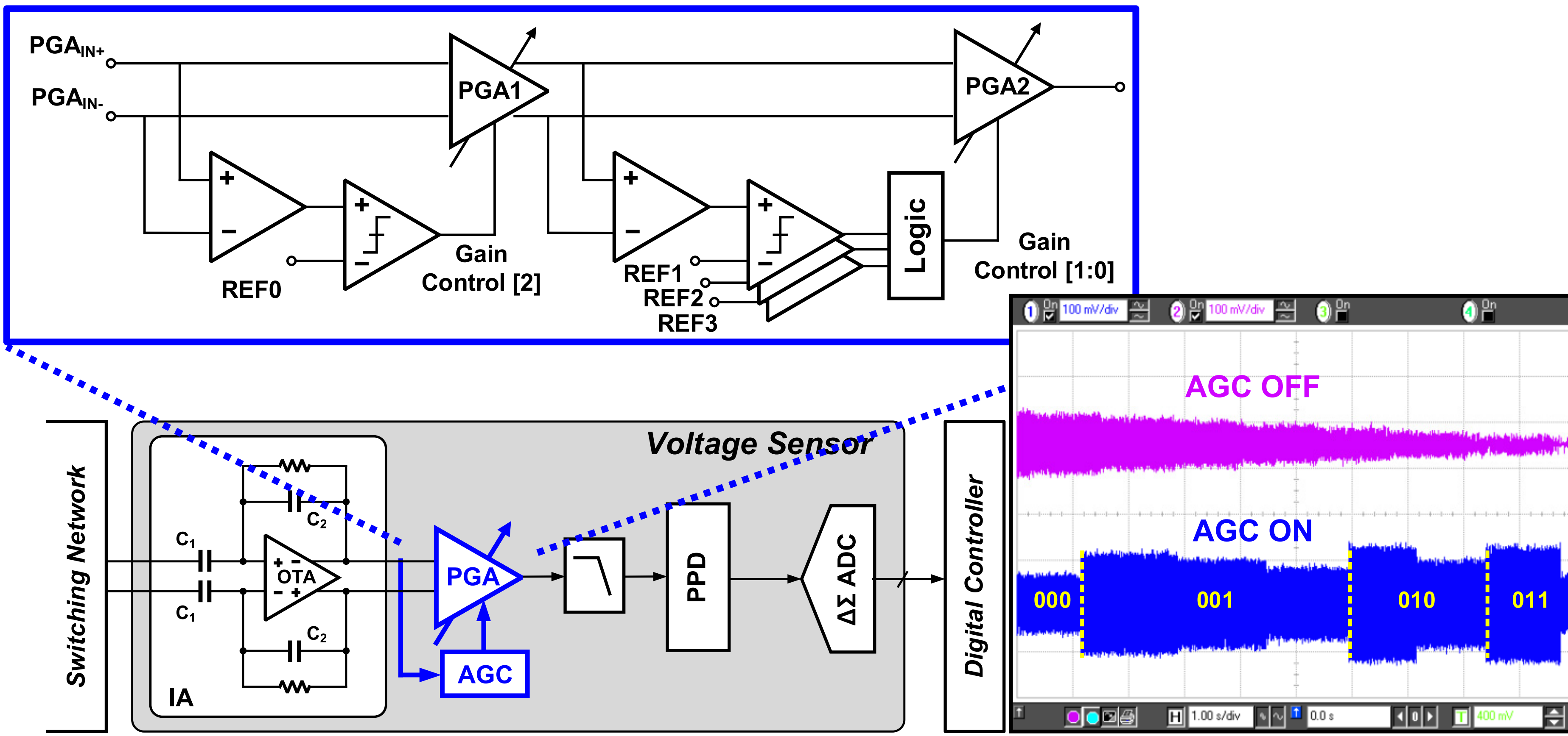
Voltage Sensor

- Capacitive-coupled IA
  - Gain = C_1/C_2 = 18dB
  - Input referred noise = 35.8nV/√Hz



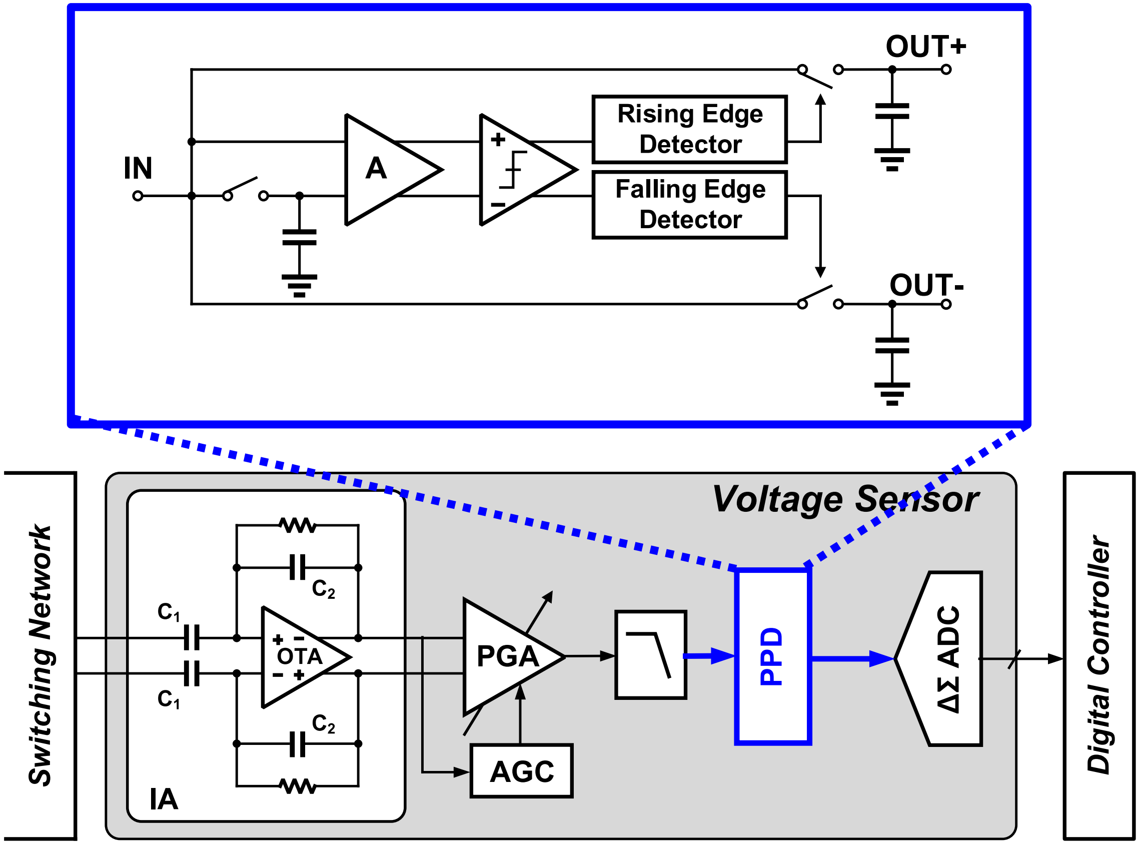
Adaptive Gain Controller (AGC)

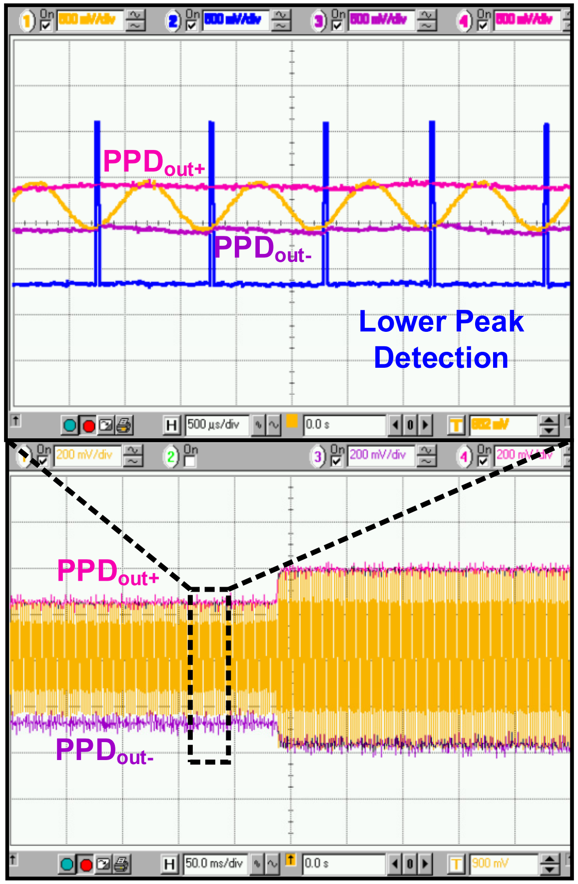
- ❑ 3-bit gain control signal
  ➔ PGA gain: 0 ~ 42dB (6dB step)



Peak-to-Peak Detector (PPD)

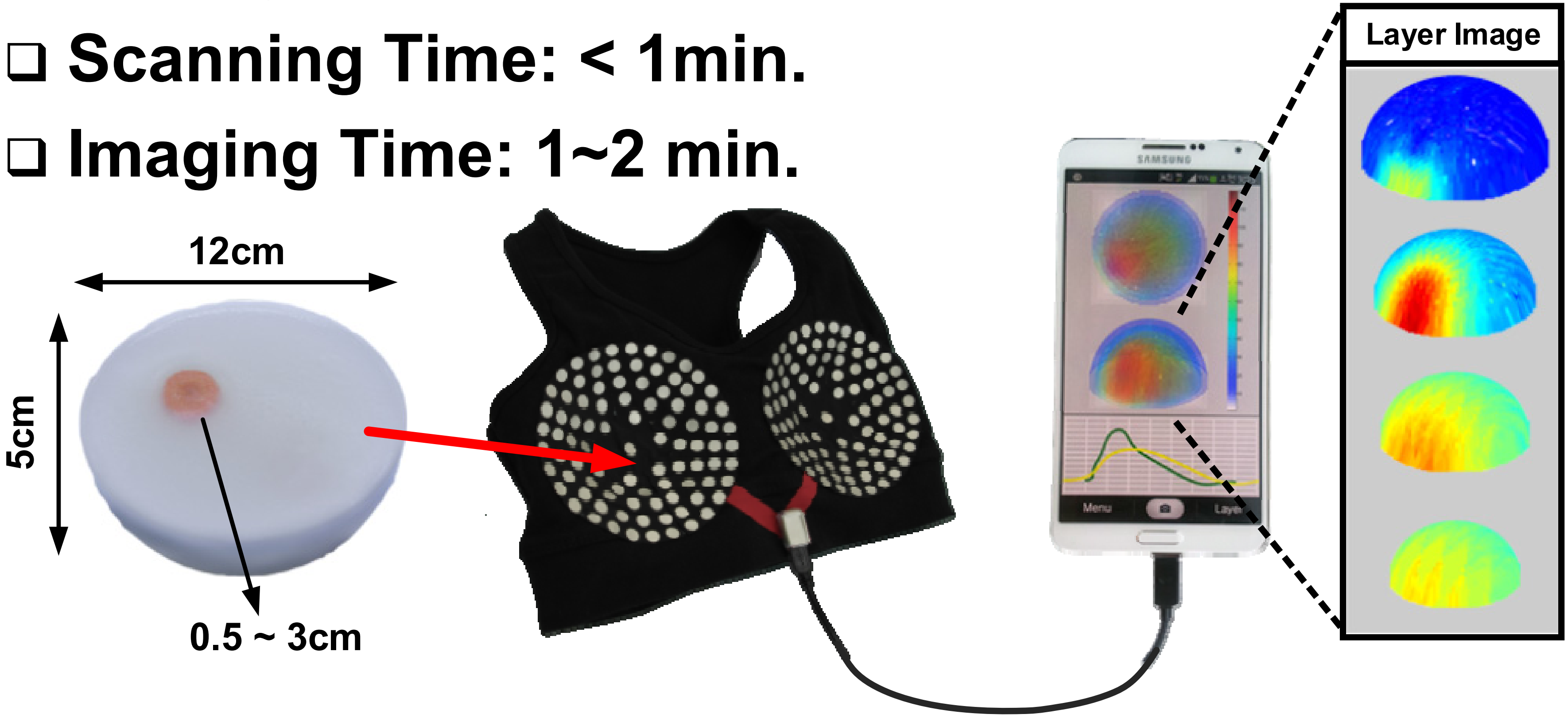
- ❑ S/H circuits to detect highest and lowest peak
- ❑ Clock freq. = 50 x input freq.



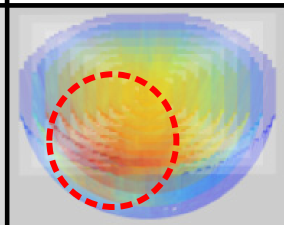
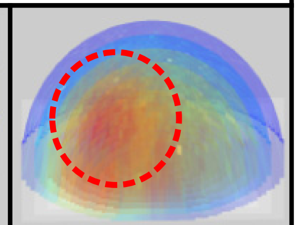
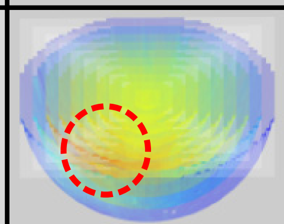
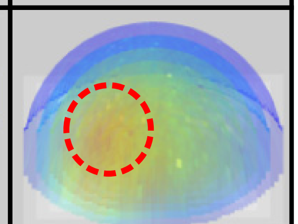
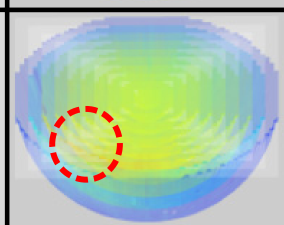
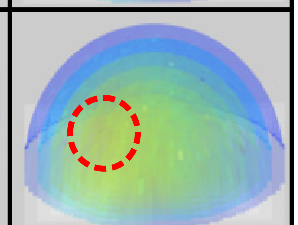


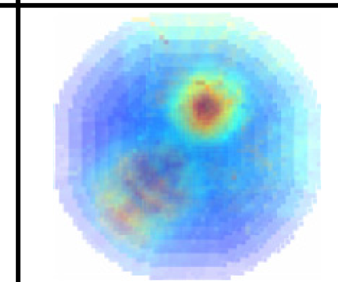
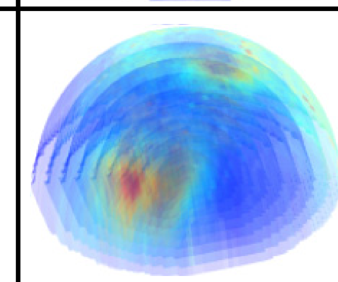
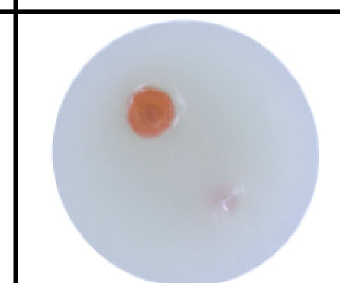
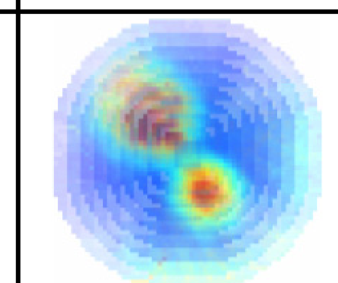
Measurement Set-up

- ❑ **Breast Model**
  - – Normal breast tissue: agar (breast-shaped)
  - – Malignant tumor: carrot
- ❑ **Scanning Time: < 1min.**
- ❑ **Imaging Time: 1~2 min.**



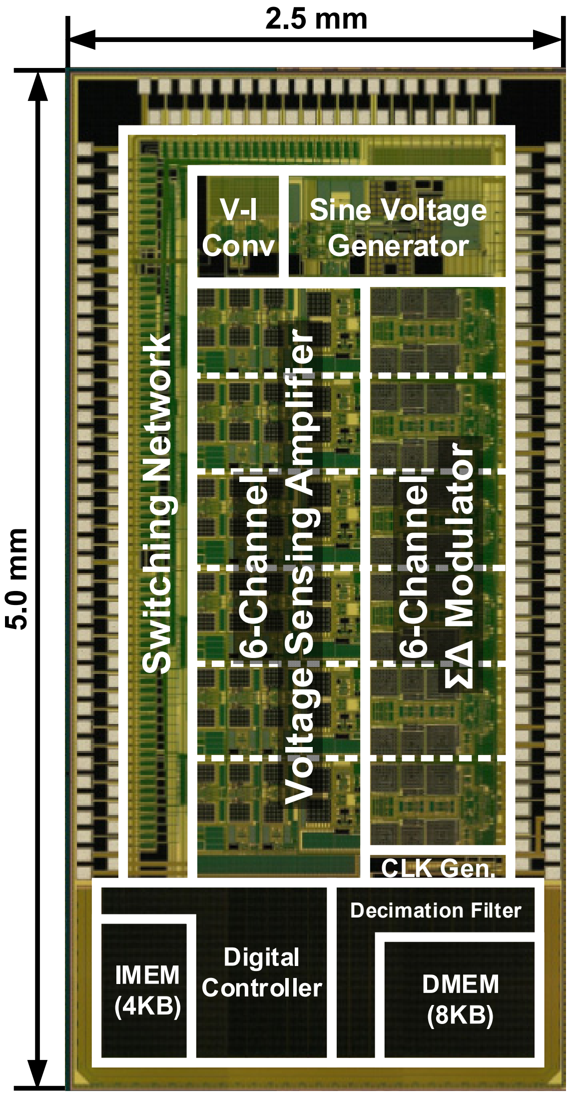
Measurement Results

Carrot Size	Model	3-D Image	
3cm			
2cm			
1cm			
1cm (X-ray)			

	Model	3-D Image
UP		
SIDE		
DOWN		

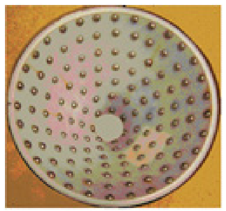
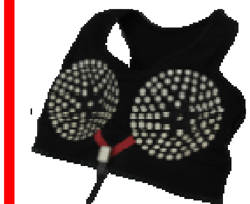
- Sensitivity: 96%, Specificity: 92%

Chip Photo & Performance Summary



Process	0.18 μm 1P6M CMOS	
Die Size	2.50 mm × 5.00 mm	
Supply Voltage	1.8 V	
Power Consumption	53.4 mW (USB supply)	
DSCS	Frequency	0.1 ~ 100 kHz (4 step)
	Amplitude	10 ~ 400 $\mu A_{p\text{-}p}$
	THD	< 0.2% @ 200 $\mu A_{p\text{-}p}$
Read-Out Front-End	# of Channels	6
	Gain	18 ~ 60 dB (6 dB step)
	Bandwidth	0.1 ~ 100 kHz
	Input Noise	36 nV/√Hz
	Sensitivity	4.9 mΩ
	ADC Clock Freq.	10 kHz ~ 40 MHz
Digital Controller	Operating Freq.	40 MHz
	On-chip SRAM	DMEM: 8 KB IMEM: 4 KB

System Comparison

System	Duke Univ.	Dartmouth	TransScan	MEIK	This Work
System Type					
	Bed	Bed	Probe + Ref. electrode	Hand-held device + Ref. electrode	Brassiere (Wearable)
Dimension	11.7 cm height, 19.1 cm diameter	60 cm diameter (Al annulus)	7.2 x 7.2 cm (electrode)	16 x 18 x 10 cm	30 x 25 x 5 cm
Weight	N/A	N/A	N/A	2 kg	72 g
Image Dimension	2D slices	3D	2D	2D slices	3D
Z_{cont} Monitoring	X	X	X	O	O
Imaging Device	Computer	Computer	Computer	Computer	Mobile Device
Electrodes	128 (7 layers)	64 (4 layers)	256 (planar)	256 (planar)	92 (Flexible)
Frequency	n/a	10 kHz - 10 MHz	58 Hz - 5 kHz	10 kHz, 50 kHz	100 Hz - 100 kHz
Amplitude	1 mA	N/A	1 ~ 2.5 V	0.5 mA	10 µA ~ 400 µA

Conclusion

- The first wearable early breast cancer detection system is implemented
  - Fabric electrode array ➔ Stable electrode contact
  - Fully integrated EIT IC ➔ Small, light form factor
  - Imaging with smart device ➔ Easy to use
- 3 operation mode & High performance EIT IC
  - ➔ 4.9mΩ sensitivity of impedance difference
  - ➔ Harmonics of stimulation current < -59dBc

Achieve compact and convenient early breast cancer detection system

A 2.14mW EEG Neuro-feedback Processor with Transcranial Electrical Stimulation for Mental Health Management

Taehwan Roh, Kiseok Song, Hyunwoo Cho, Dongjoo Shin,
Unsoo Ha, Kwonjoon Lee
and Hoi-Jun Yoo

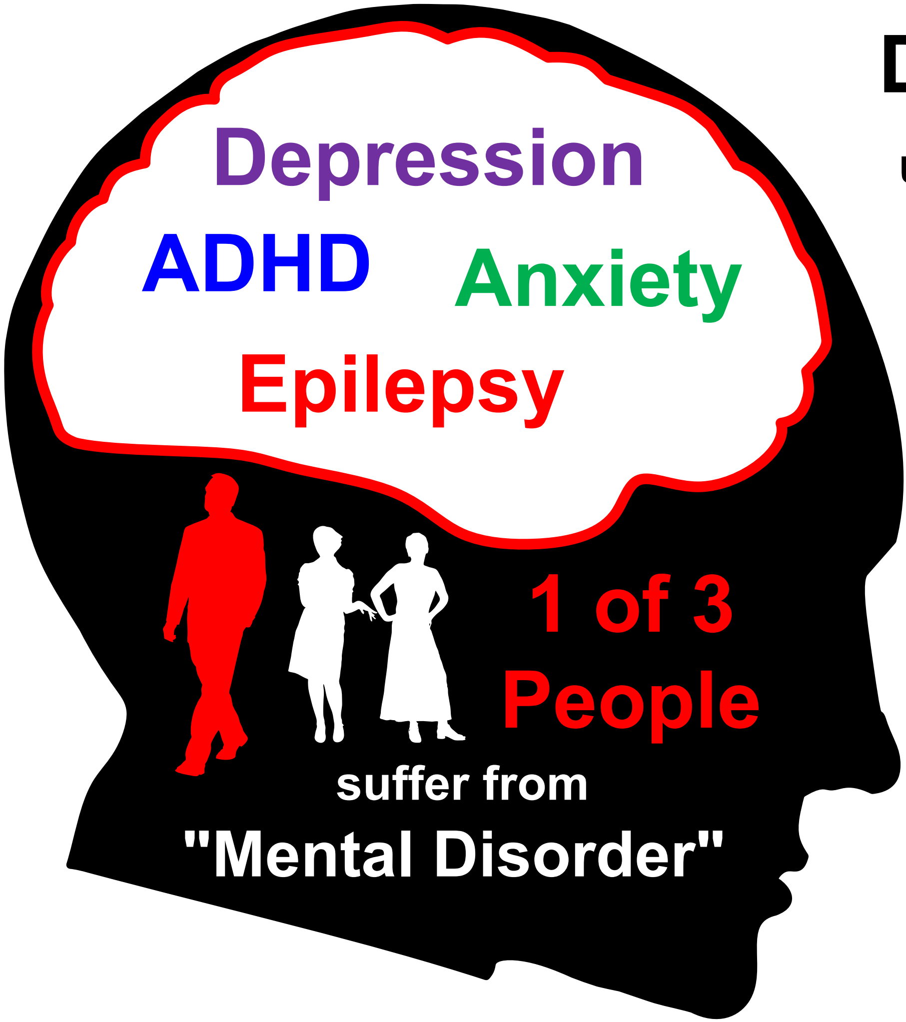
Semiconductor System Laboratory

Dept. of EE, KAIST

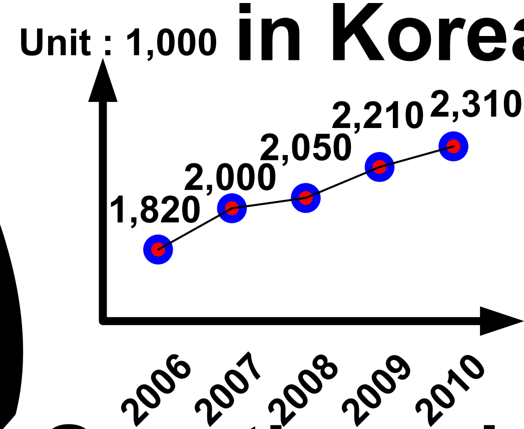
Outline

- ❑ **Introduction**
- ❑ **Neuro-feedback System Architecture**
- ❑ **Key Building Blocks**
  1. Mental Health Monitoring Accelerators
     I. Dimension Reduction with Source Selection
     II. Accelerators for Component Decomposition
  2. Programmable Electrical Stimulator (PES)
- ❑ **Case Study with Hospital**
- ❑ **Conclusion**

What is Mental Health?



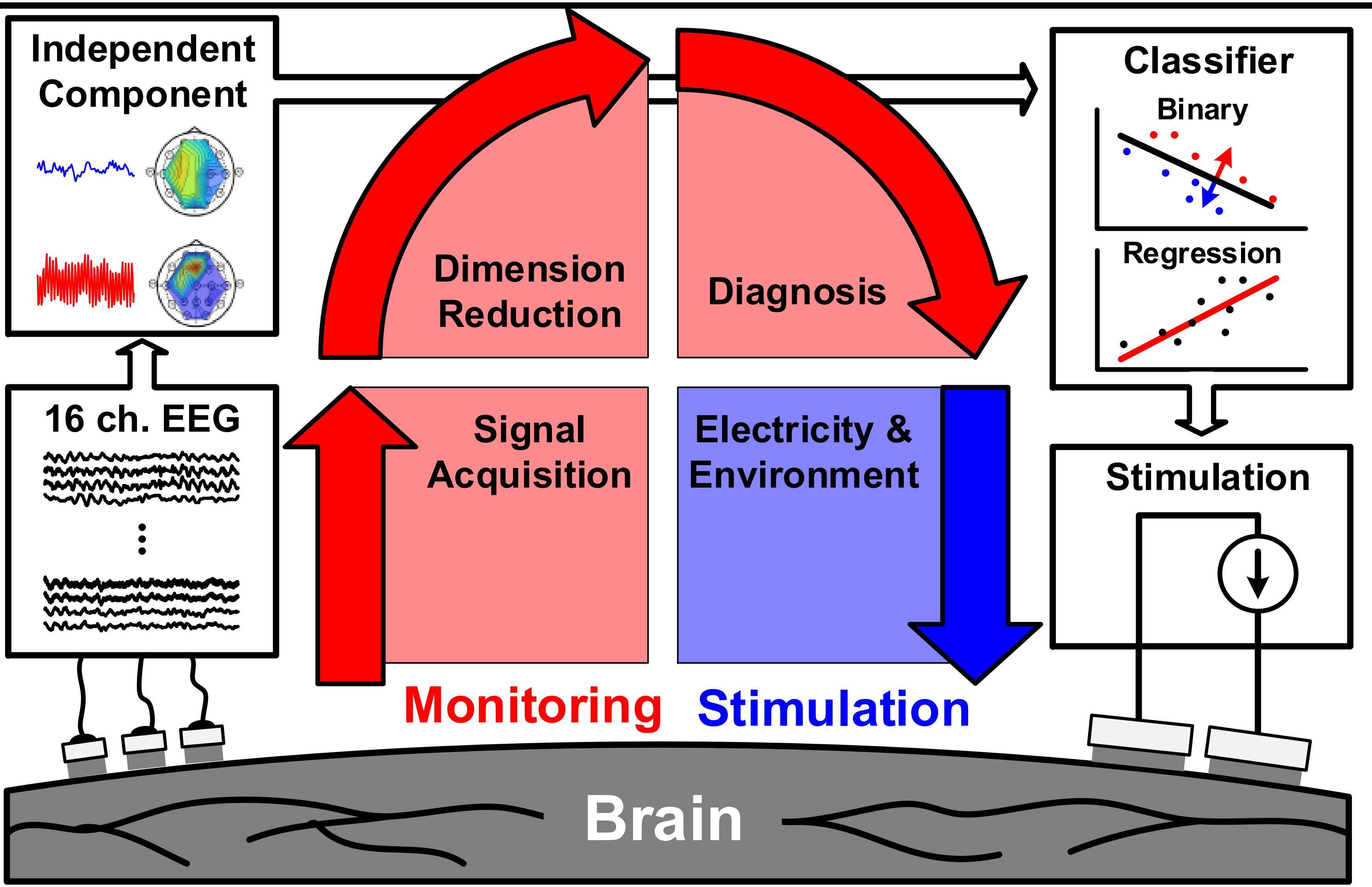
Depression Patients in Korea



Questionnaire-based Diagnosis

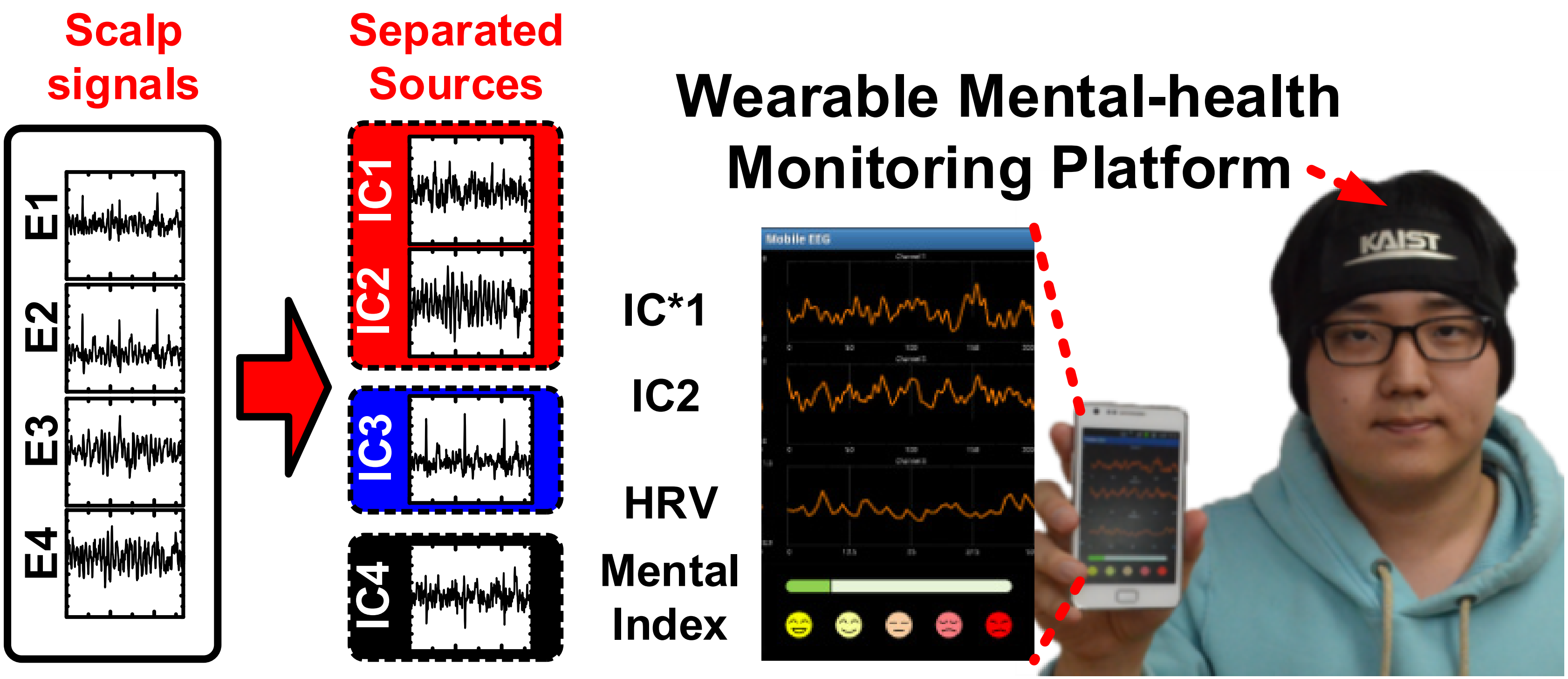
Diagnostic and Statistical Manual of Mental Disorders, Fifth Edition

Mental Health Management



Previous System : Smart Headband

- 4 Channel Sensor → Diagnosis in Smart Dev.
- Low Cost w/ Fast Temporal Resolution

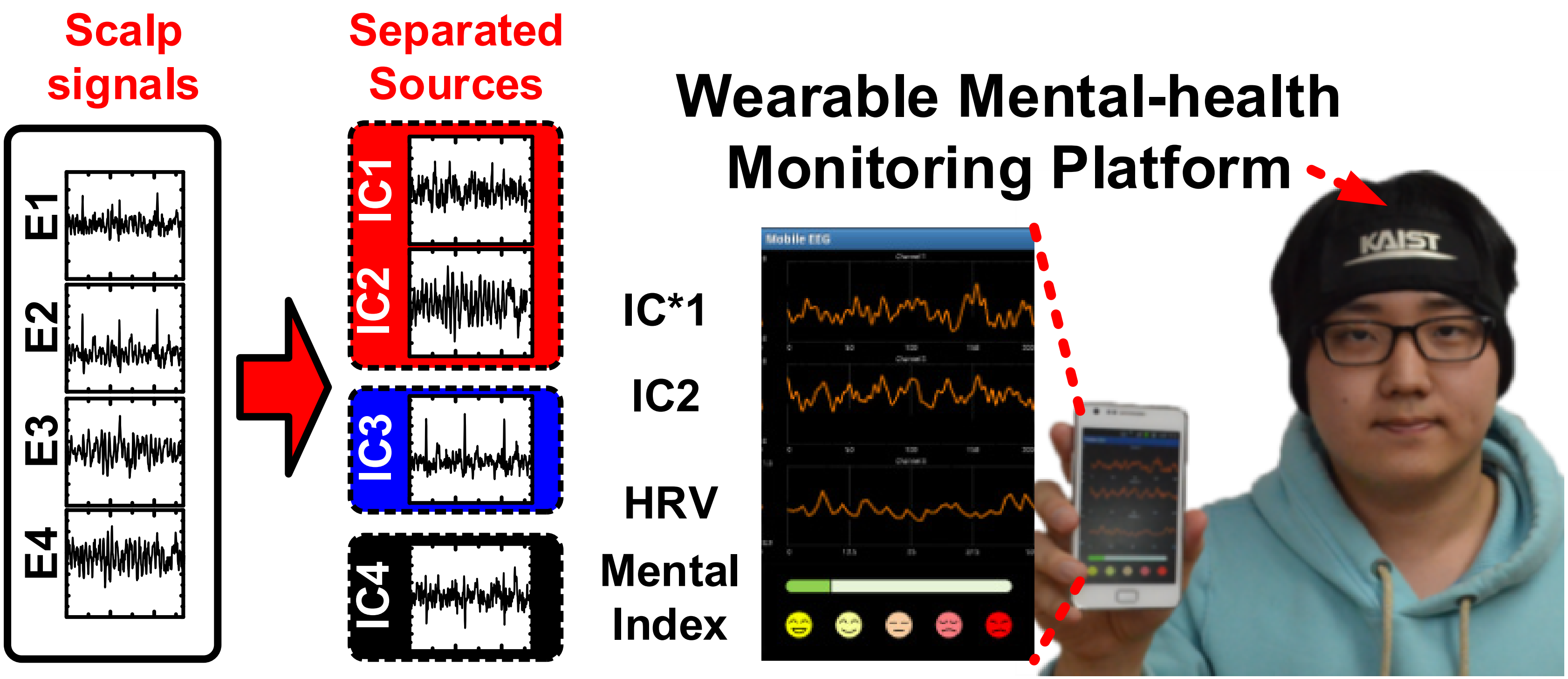


IC : Independent Component

T. Roh, ISSCC 2012

Weakness : Smart Headband

- ❑ **No Online Artifact Removal on Chip**
- ❑ **No Therapeutic Procedure**



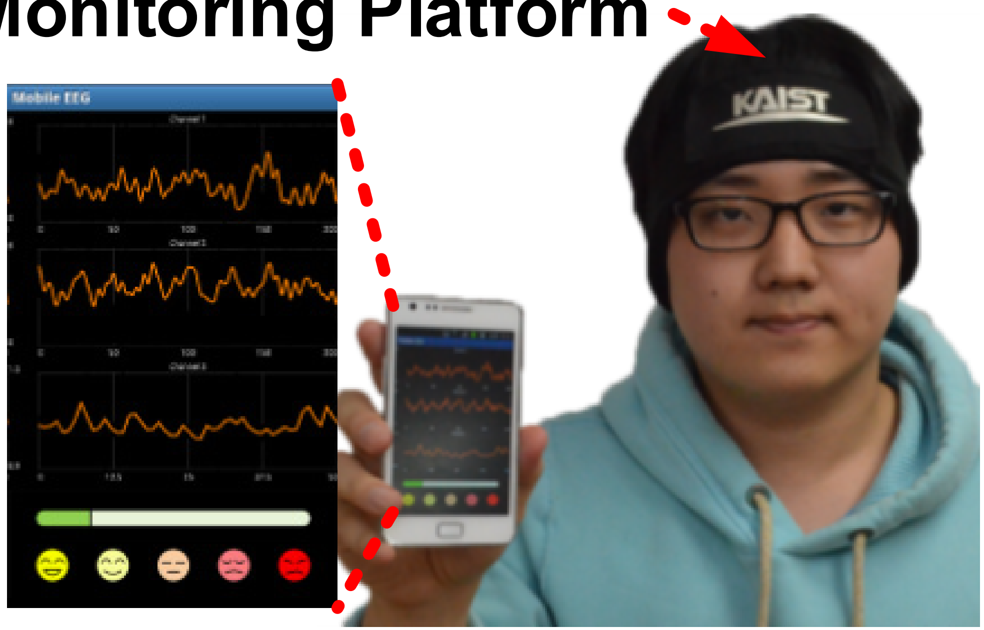
IC : Independent Component

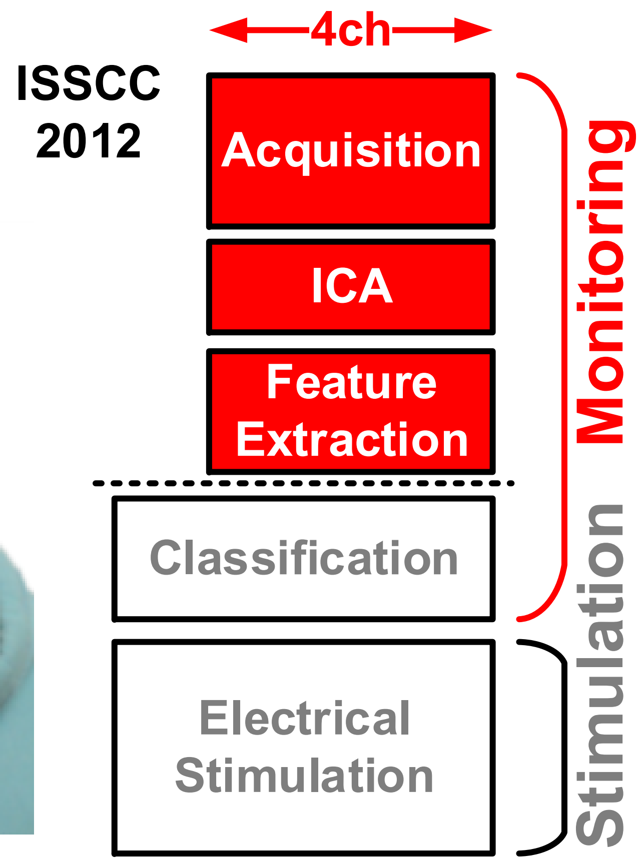
T. Roh, ISSCC 2012

Previous System Overview

❑Mental Health Monitoring System

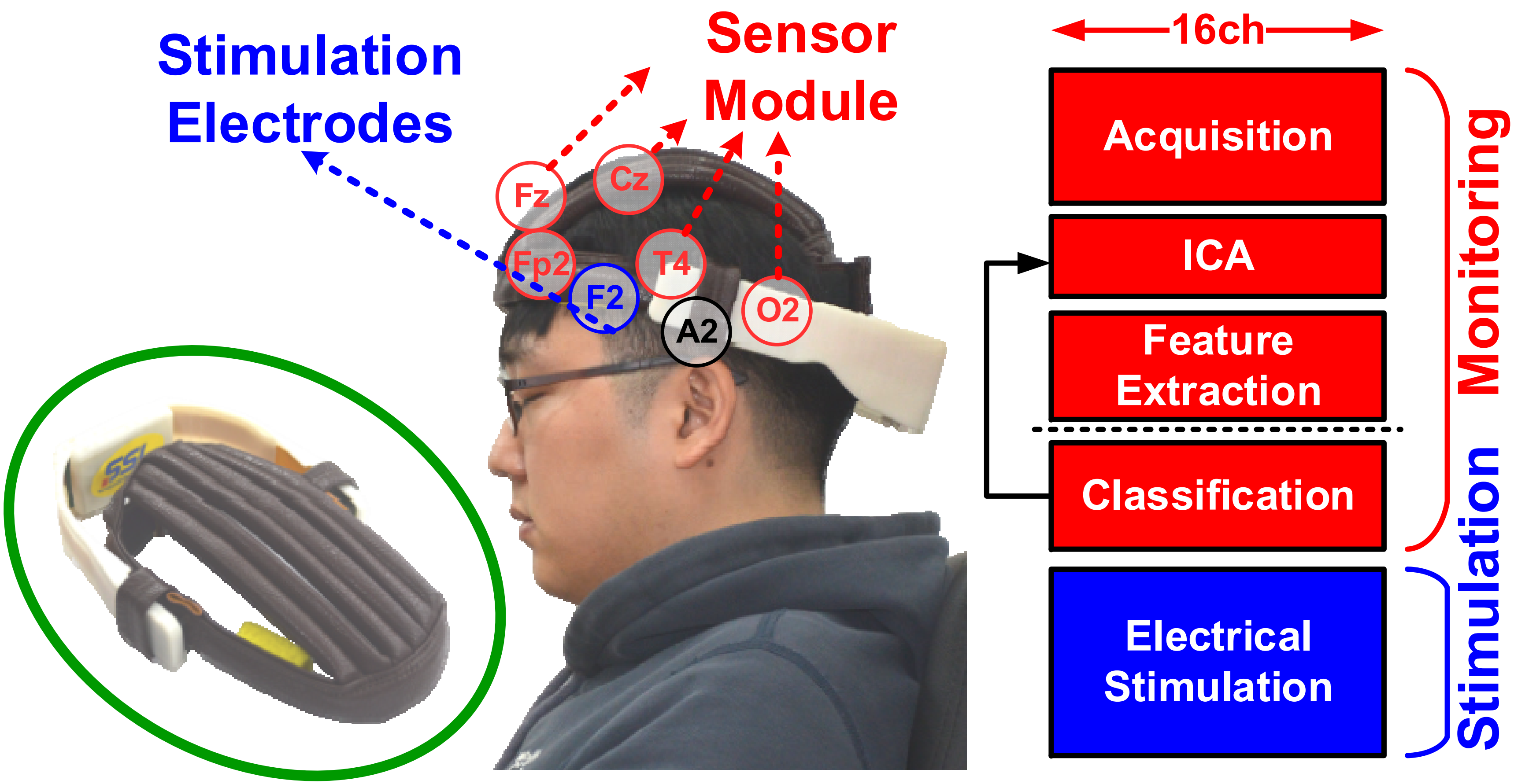
Wearable Mental-health Monitoring Platform





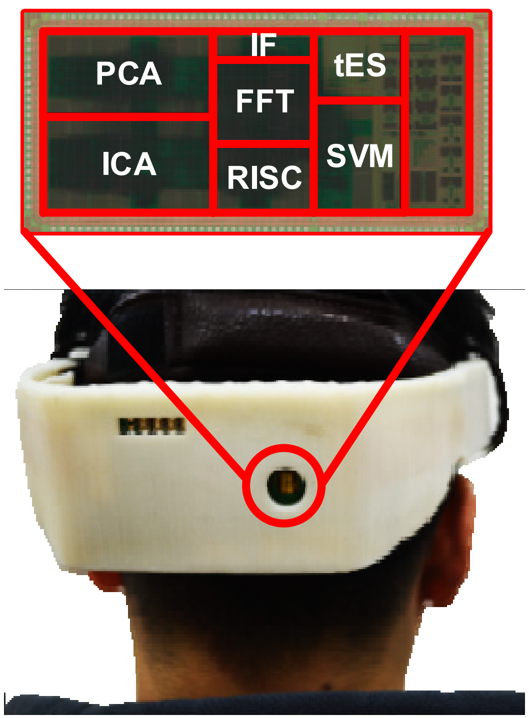
Proposed System Overview

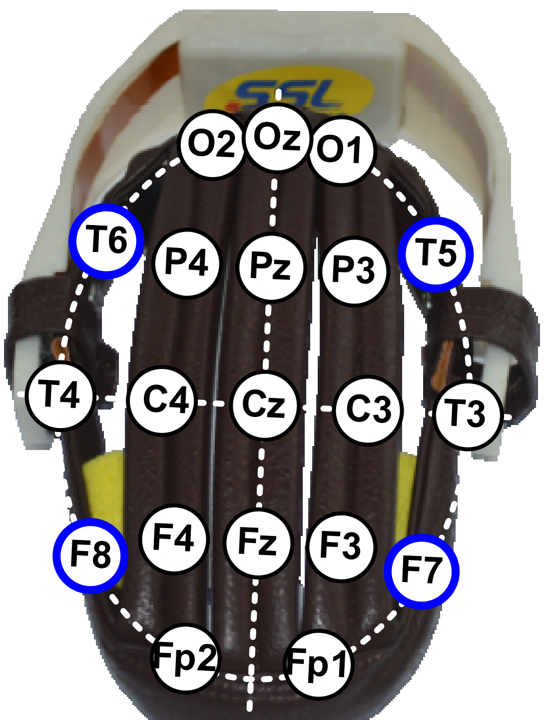
❑Neuro-Feedback Headgear System

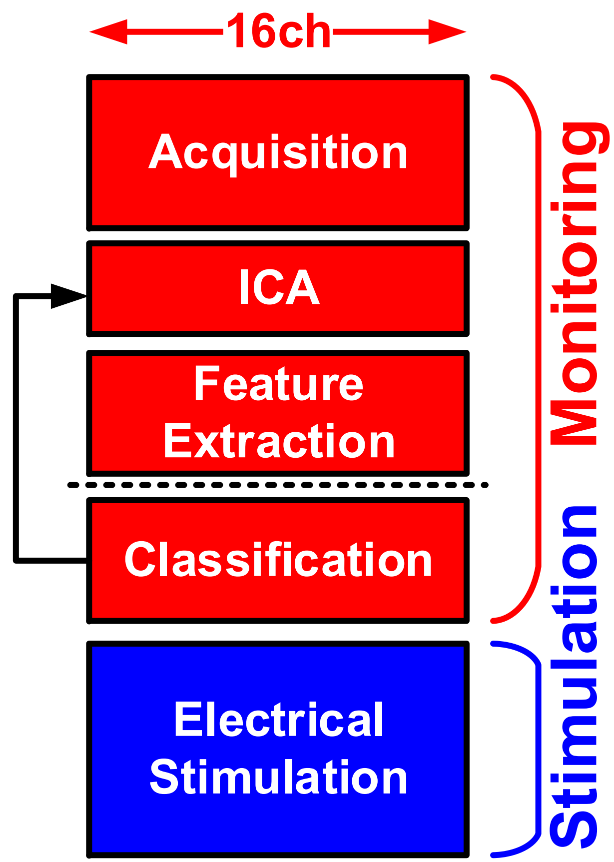


Proposed System Overview

❑Neuro-Feedback Headgear System



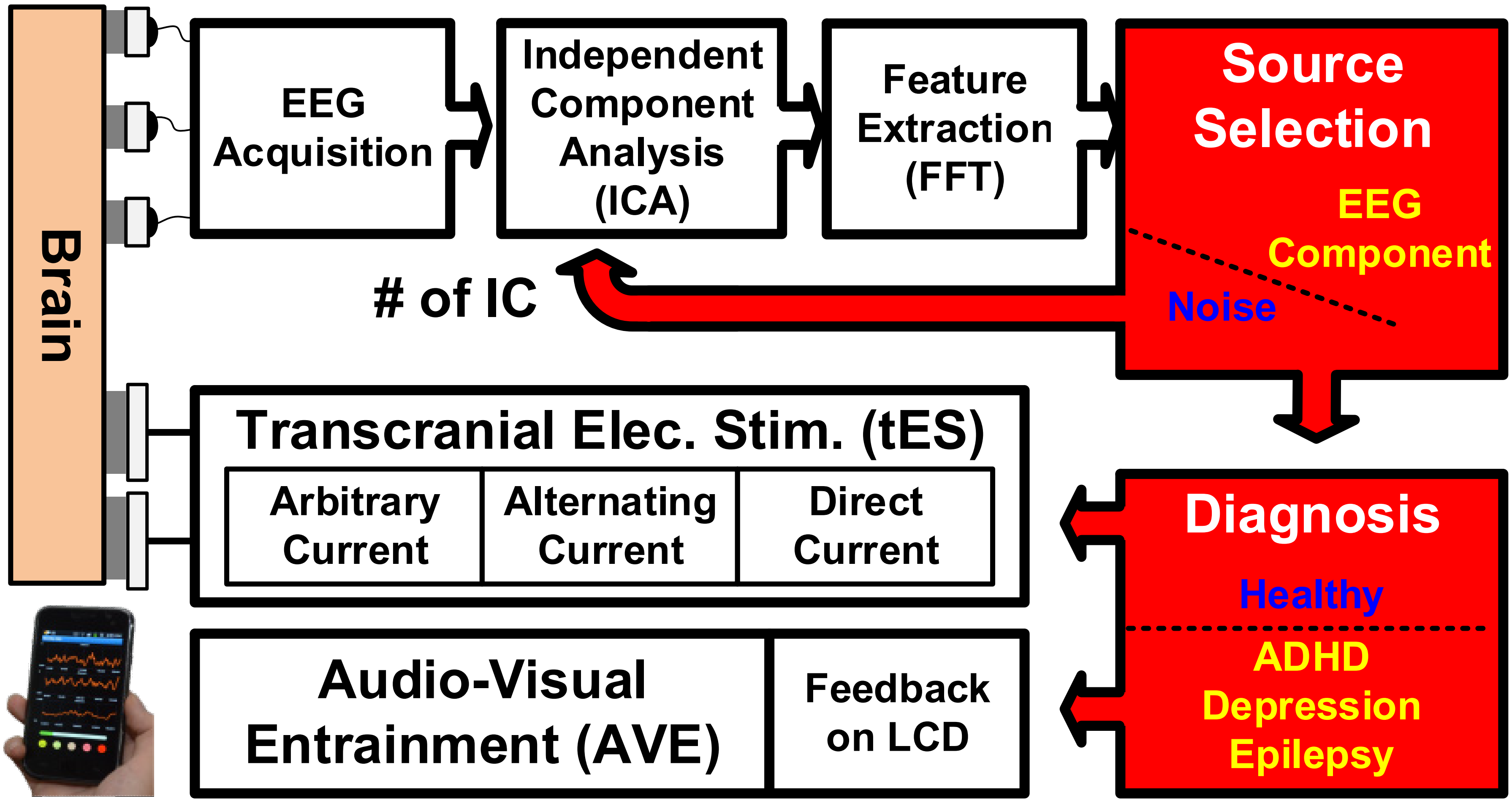




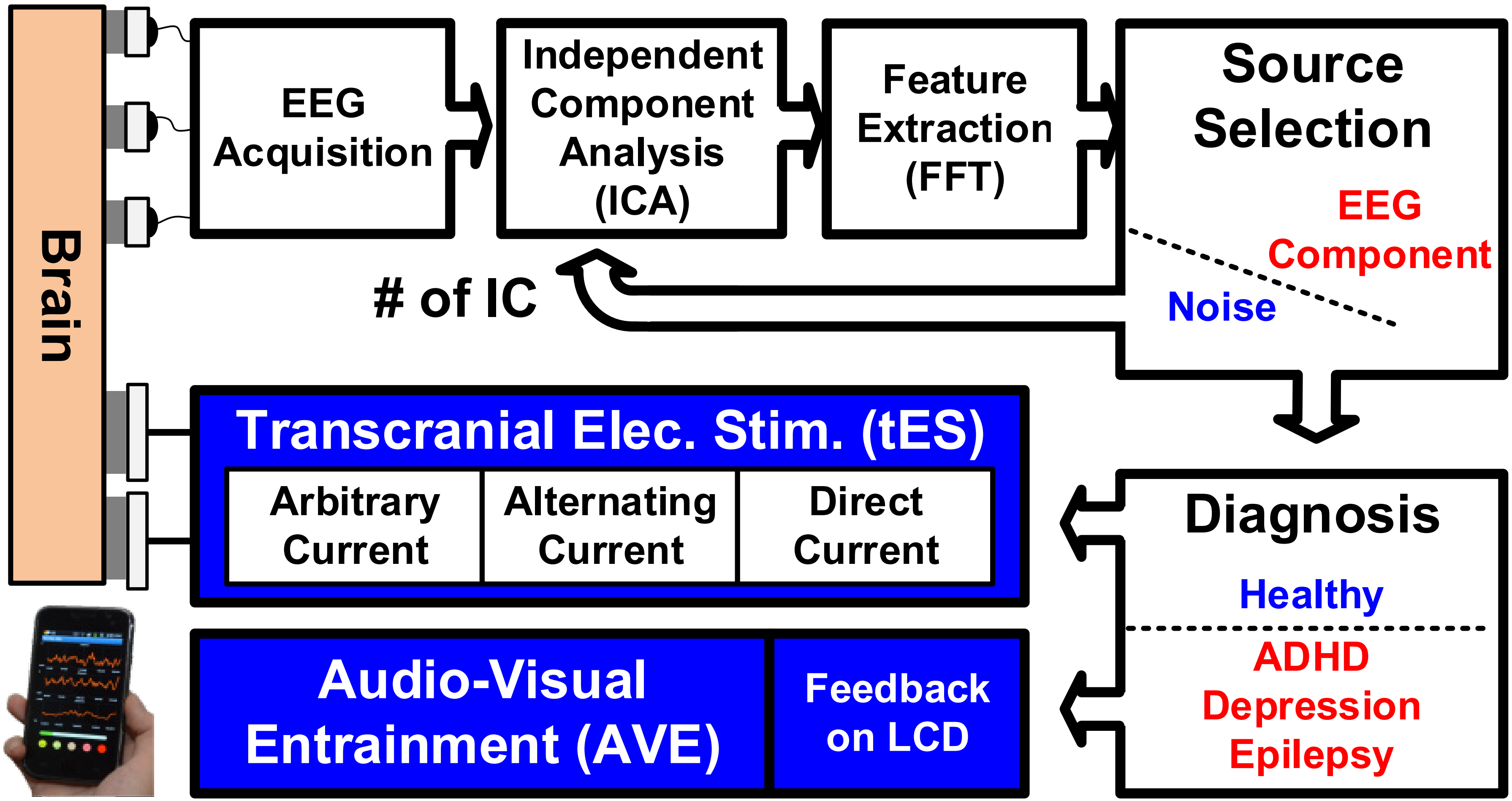
Proposed System Demonstration

Neuro-feedback Headgear
for Mental Health Management

Operating Flow - Monitoring



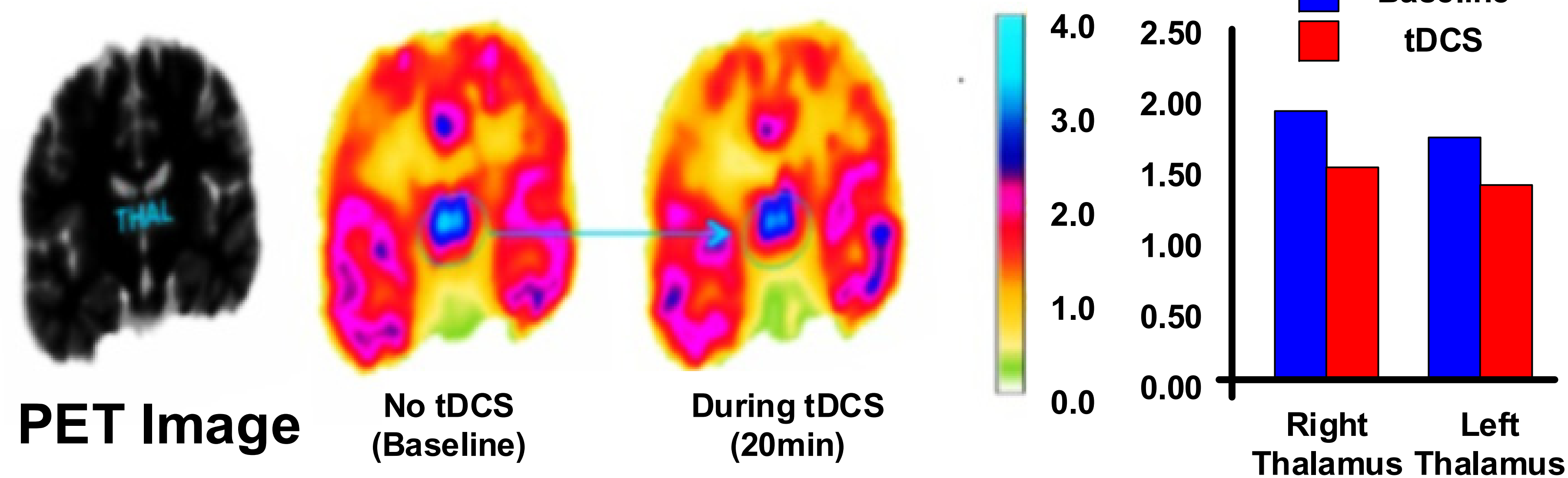
Operating Flow - Stimulation



Transcranial Electrical Stimulation (tES)

- ❑Non-invasive Treatment (Neuro-modulation)
  - – Anode-, Cathode-electrodes
  - – Non-intensive Current Stimulation (DC, AC)

Decrease in Thalamus During 2mA tDCS Motor Cortex



Dos Santos, Marcos Fabio, et al. **"Immediate Effects of tDCS on the µ-Opioid System of a Chronic Pain Patient."** *Frontiers in Psychiatry* 3 (2012).

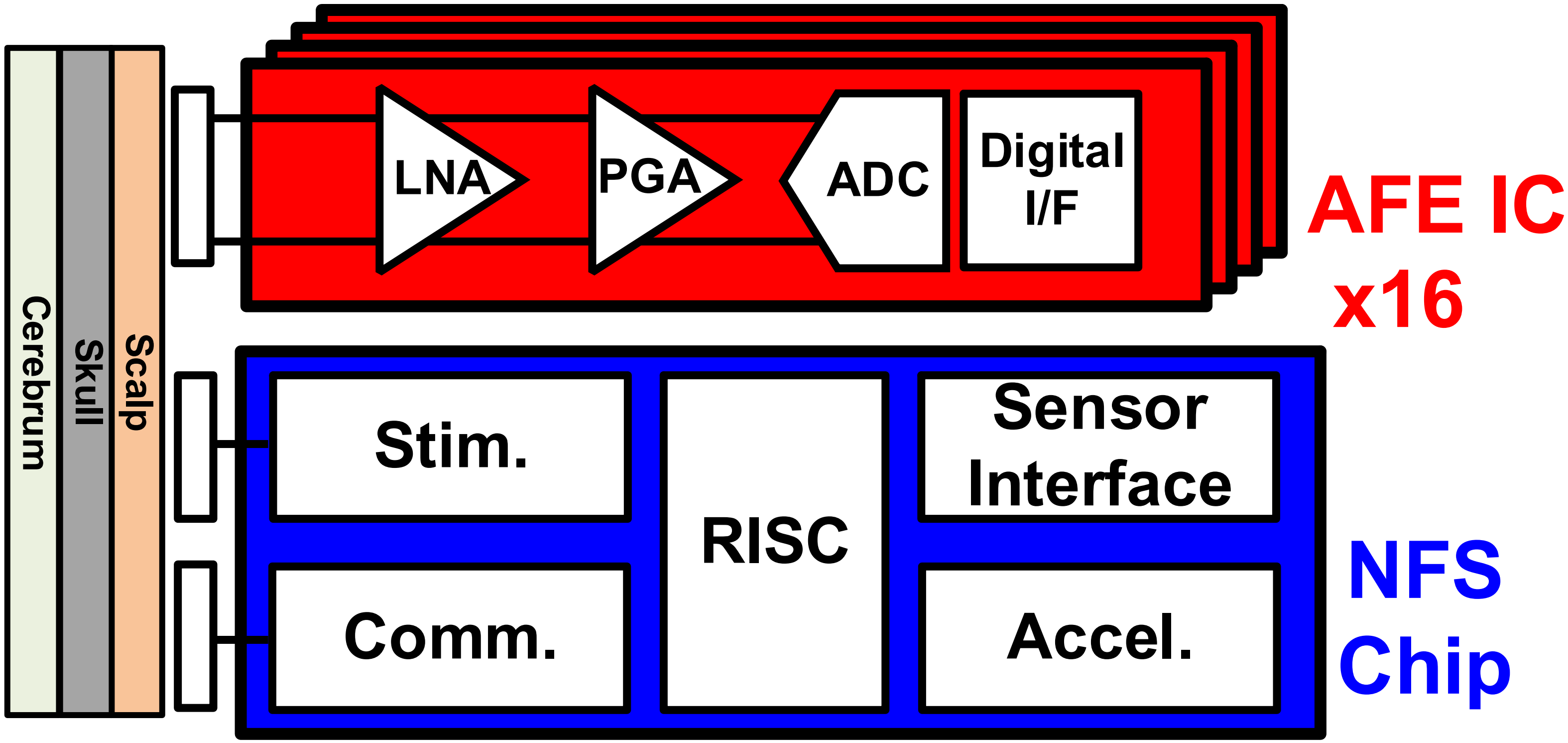
Features of Proposed System

- **Mental Health Monitoring**
  - ICA w/ 91 % of Correct Source Selection
    ➔ Reduction of Dimension & Computation
  - Pipelined Operation ➔ 34% Time Saving

- **Brain Stimulation Therapies**
  - Programmable Electrical Stimulator (PES)
    ➔ Arbitrary Waveform
    ➔ Fully support of tES (tDCS and tACS)

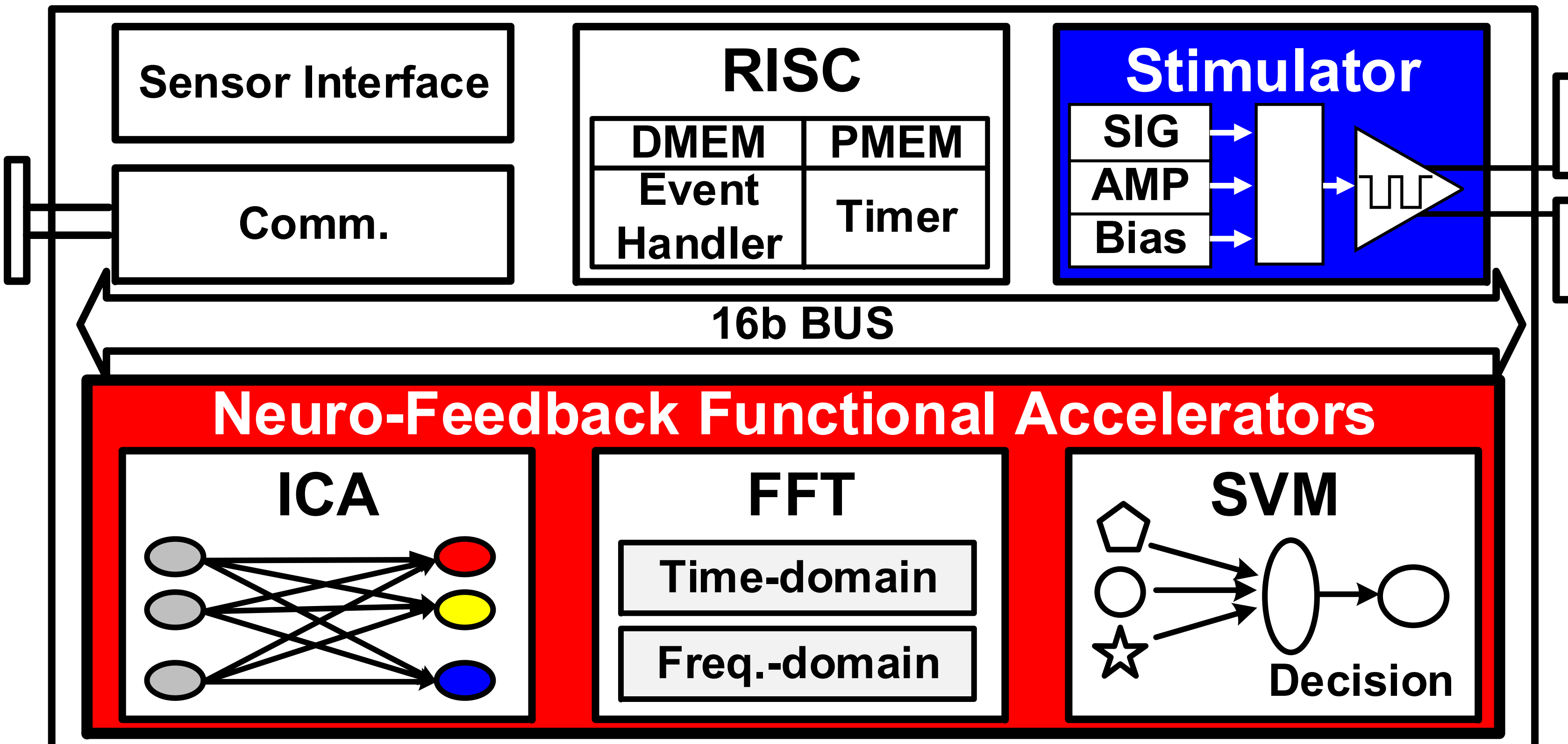
System Architecture

- 16 AFE IC → PGA, 10b ADC & Digital I/F
- Neuro-feedback SoC (NFS)



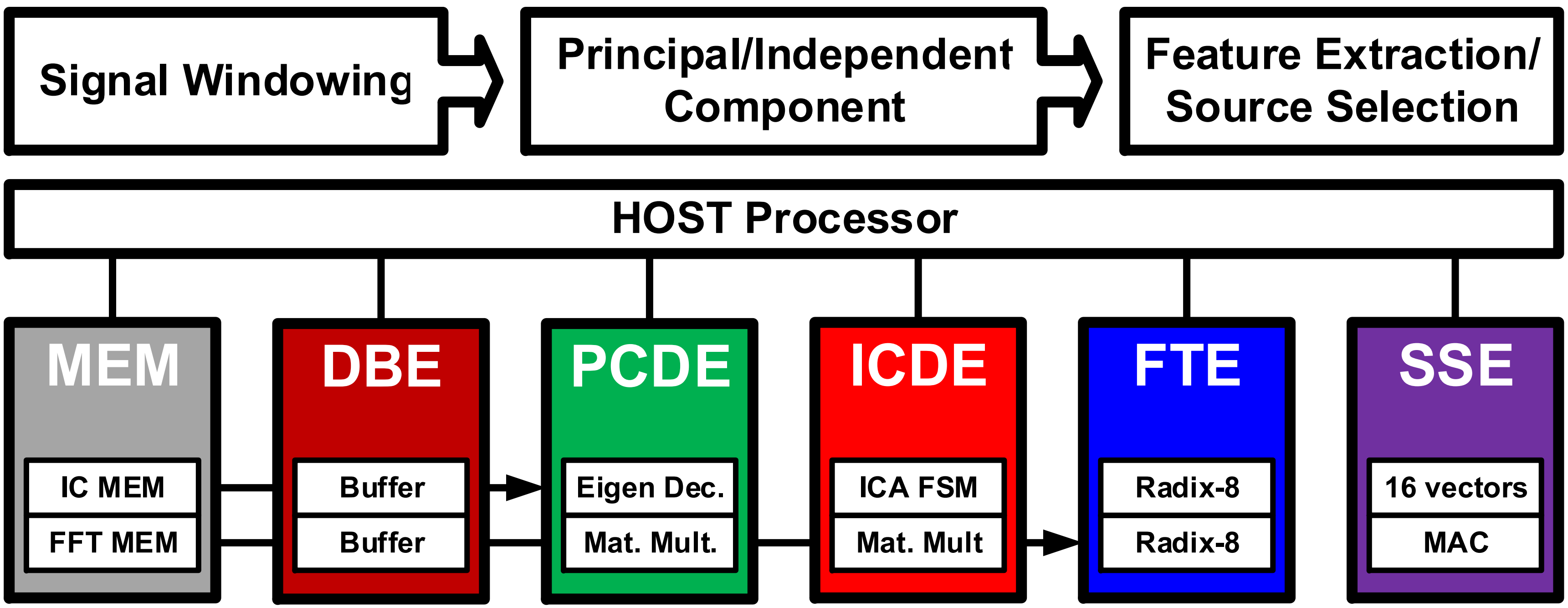
NFS Chip Architecture

- ❑ Monitoring Accelerators for Diagnosis
- ❑ Electrical Stimulator for Therapy



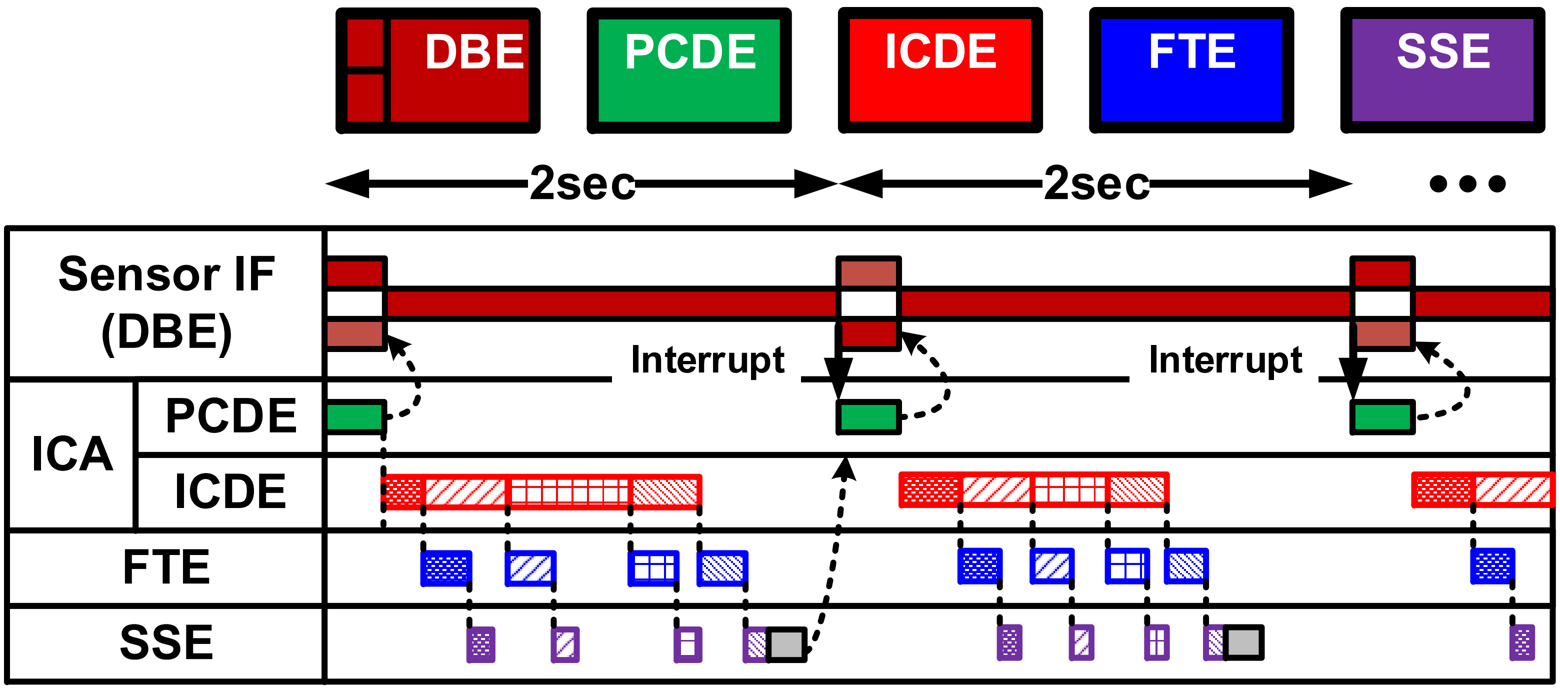
Operating Flows in Accelerators

- **5 Pipelined Operation → 5 Accel-Engines**
  - DBE : Double Buffered Engine
  - PCDE & ICDE : Component Decomposition Eng.
  - FTE & SSE : Feature & Classification Eng.



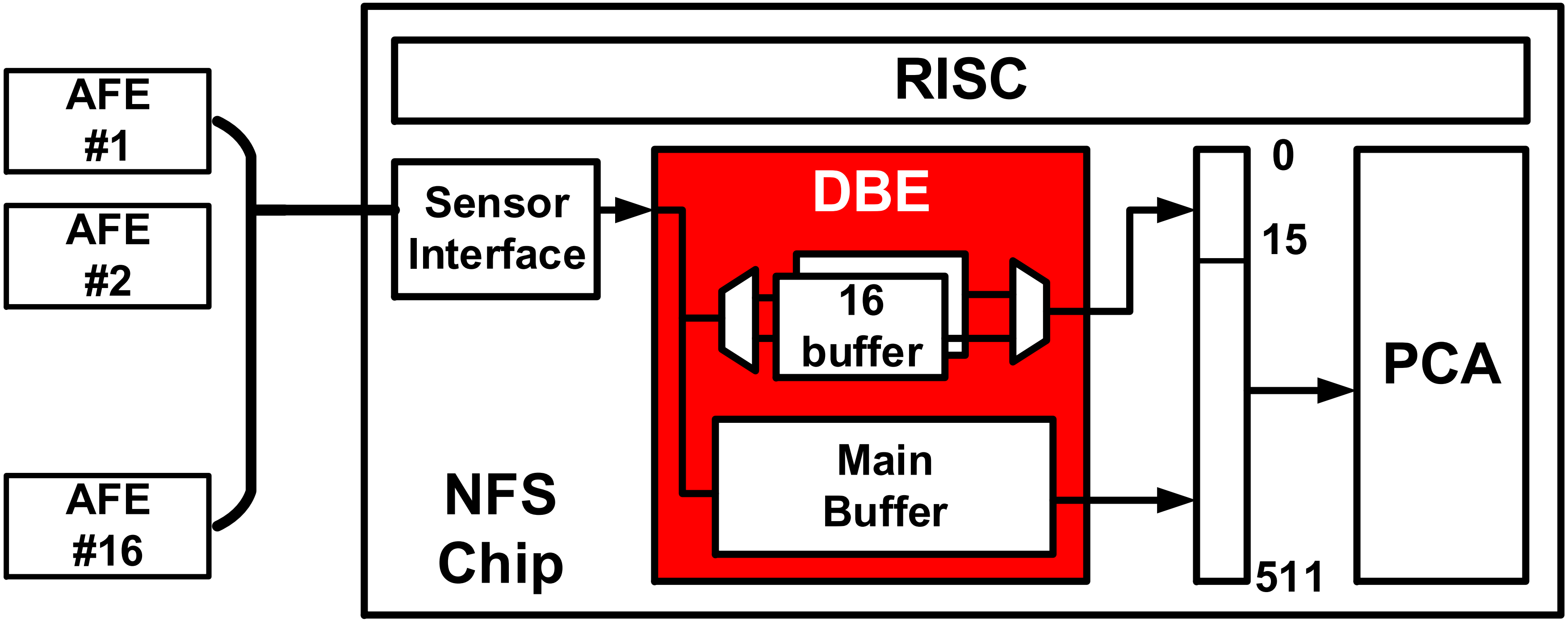
Pipelined Operation

- 5 Stage Pipeline
  - 34% of Overall Time is Saved
  - PCDE : 64ms / ICDE + FTE + SSE : 2s @ 250S/s



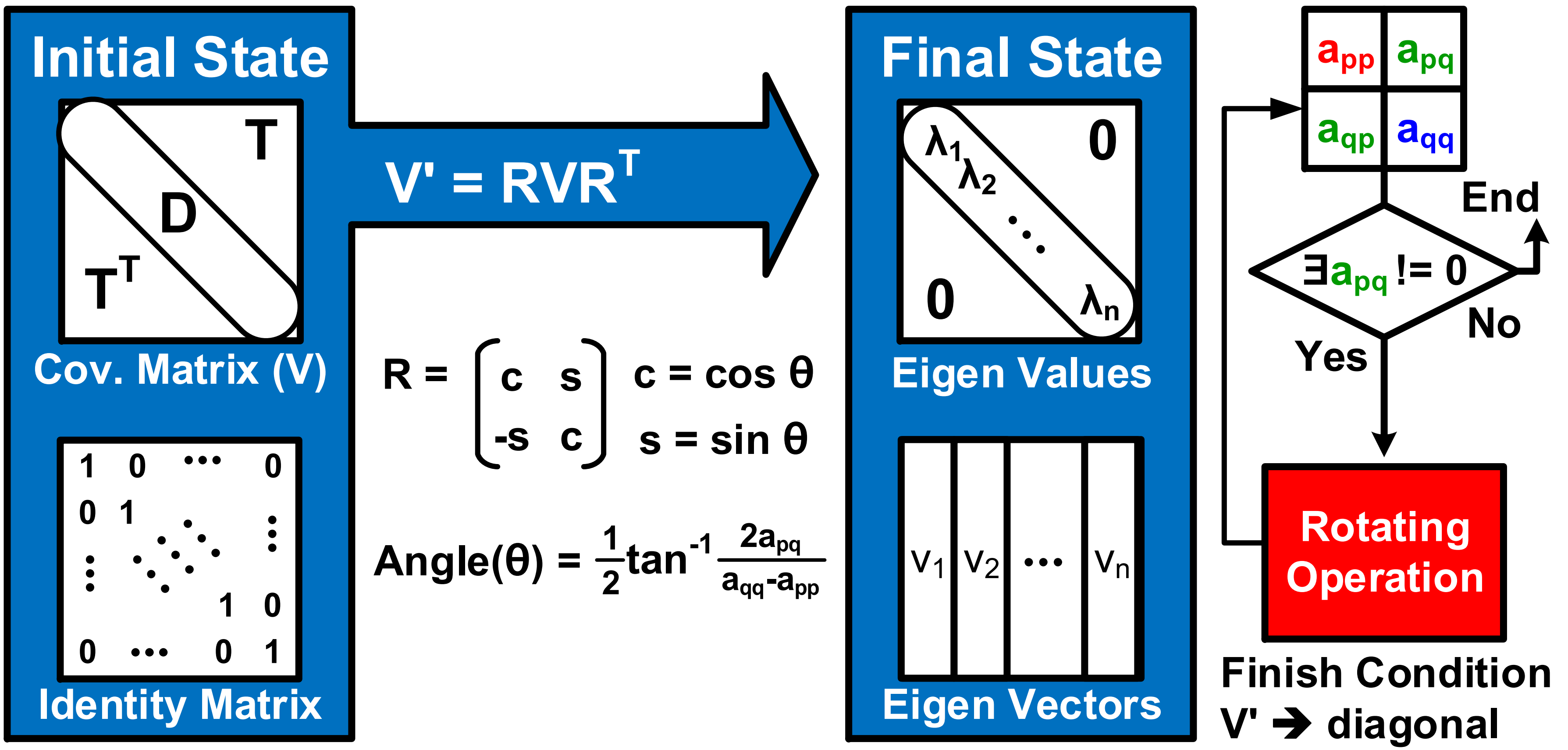
Double Buffering Engine (DBE)

- 512-depth Signal Window
- Double 16-words Sub Buffer for PCDE
  - Only 64ms @ 250S/s for PCA Operation



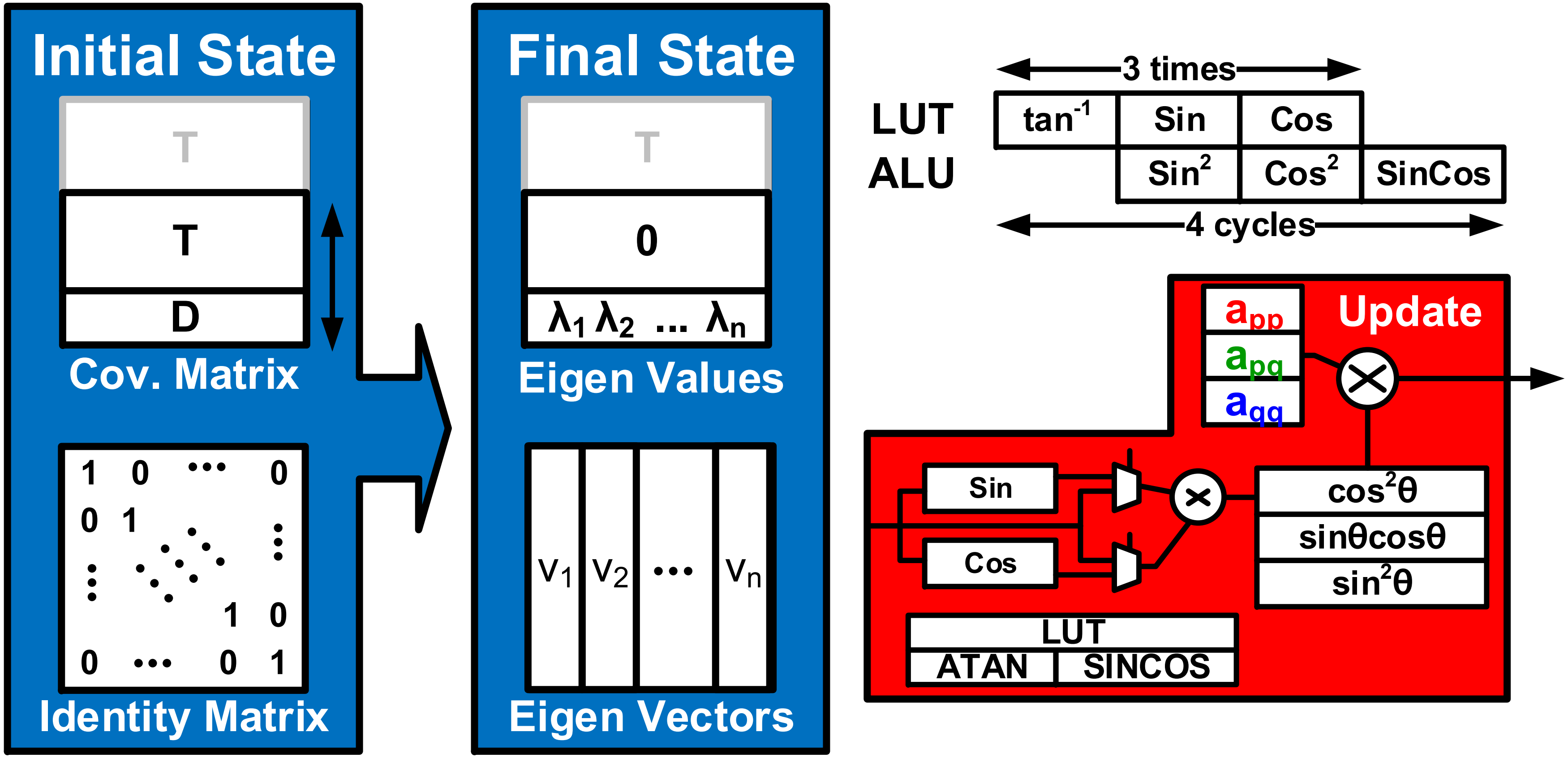
Eigen Value Decomposition in PCA

- 64ms @ 250S/s Time Slot
- EVD w/ Accelerated Rotating Operation



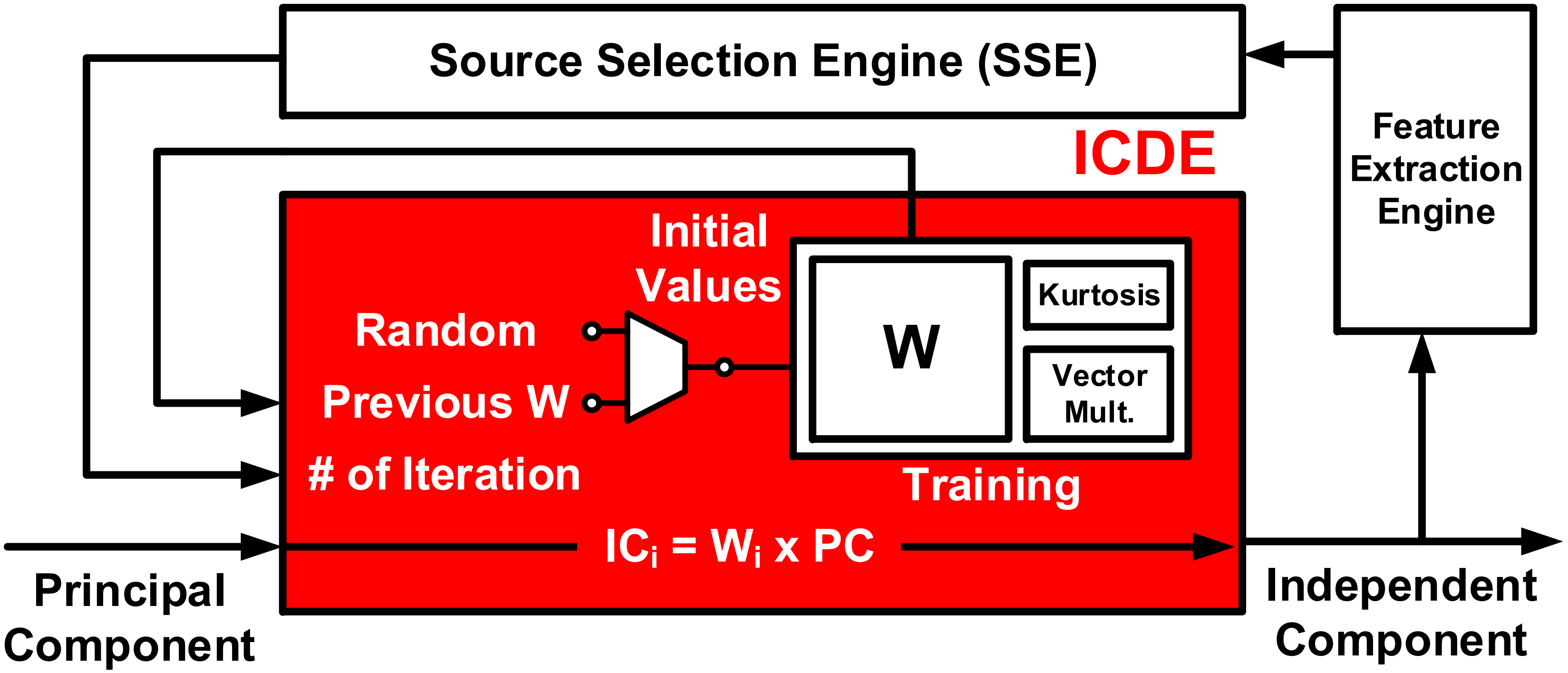
PC Decomposition Engine (PCDE)

- ❑ Sym. Matrix ➔ 23% Memory @ 16 Channel
- ❑ Look-up-table (LUT) ➔ 1 Clock for Each Tri-fun.



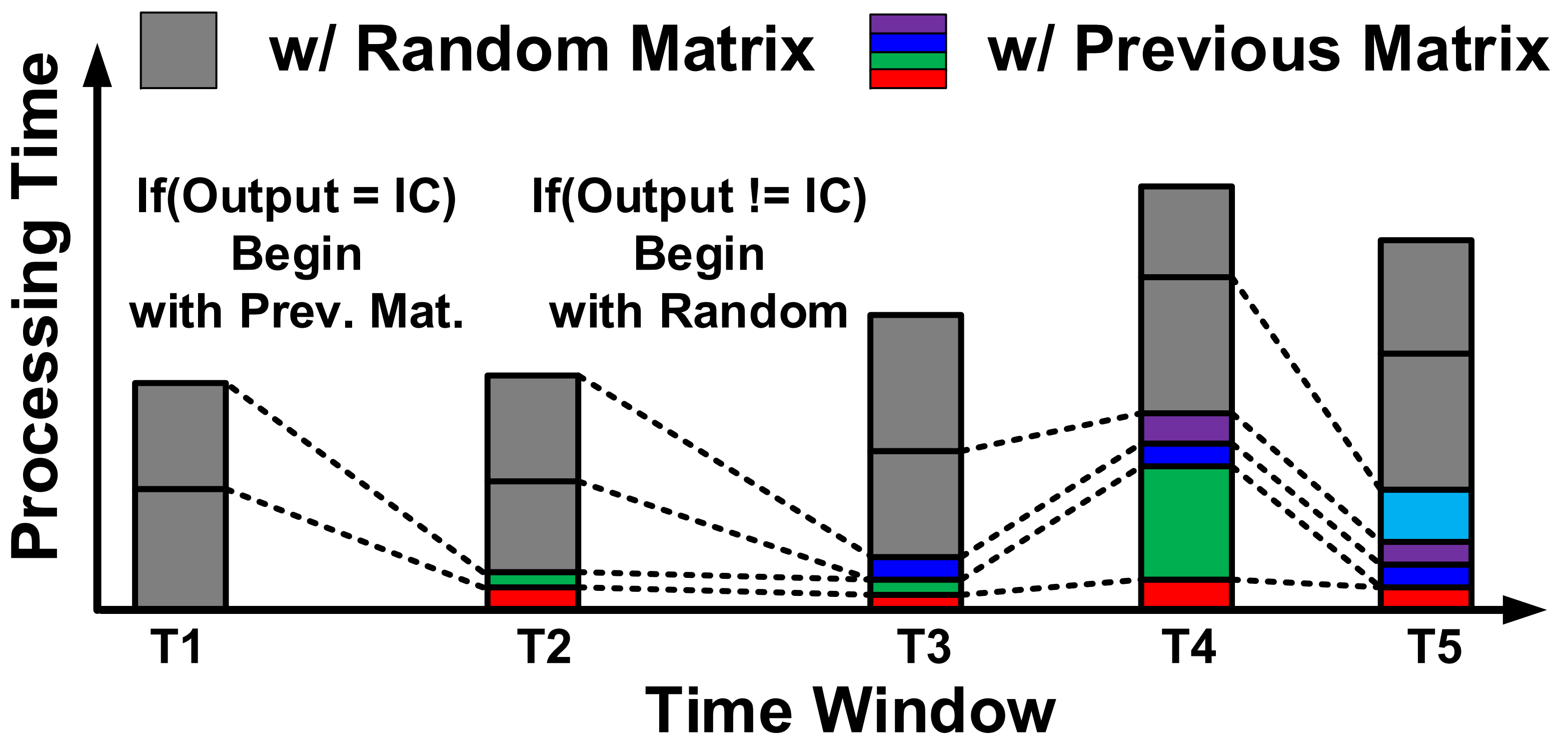
IC Decomposition Engine (ICDE)

- Parameter feedback from SSE
  - – # of ICs & Decomposition Matrix (W) in Previous



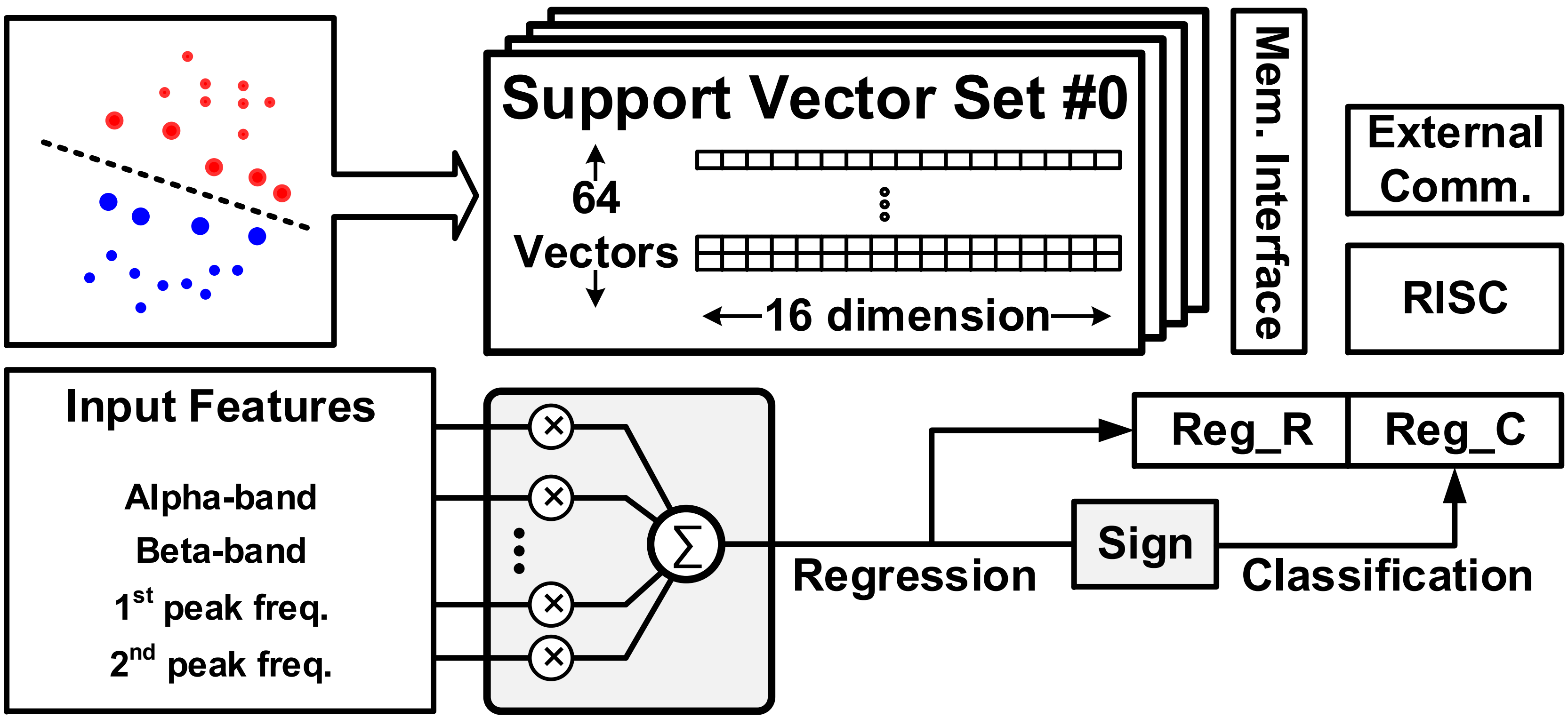
Operation of ICDE

- # of Correct Independent Components
  ➔ # of Decomposition Iterations



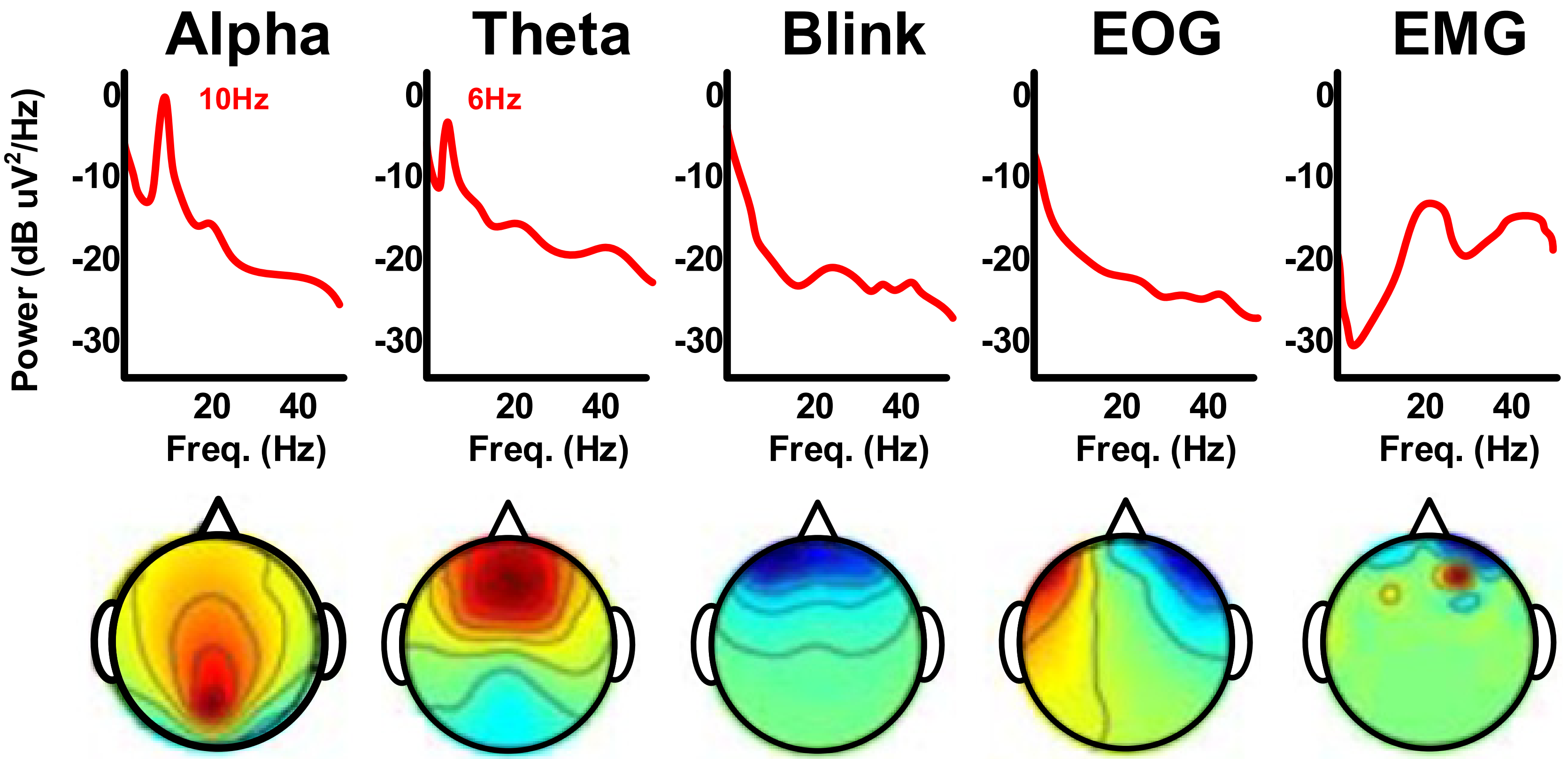
Source Selection Engine (SSE)

- ❑ 4 Different Memory Sets ➔ 4 Classification
- ❑ 91% Accurate Source Selection

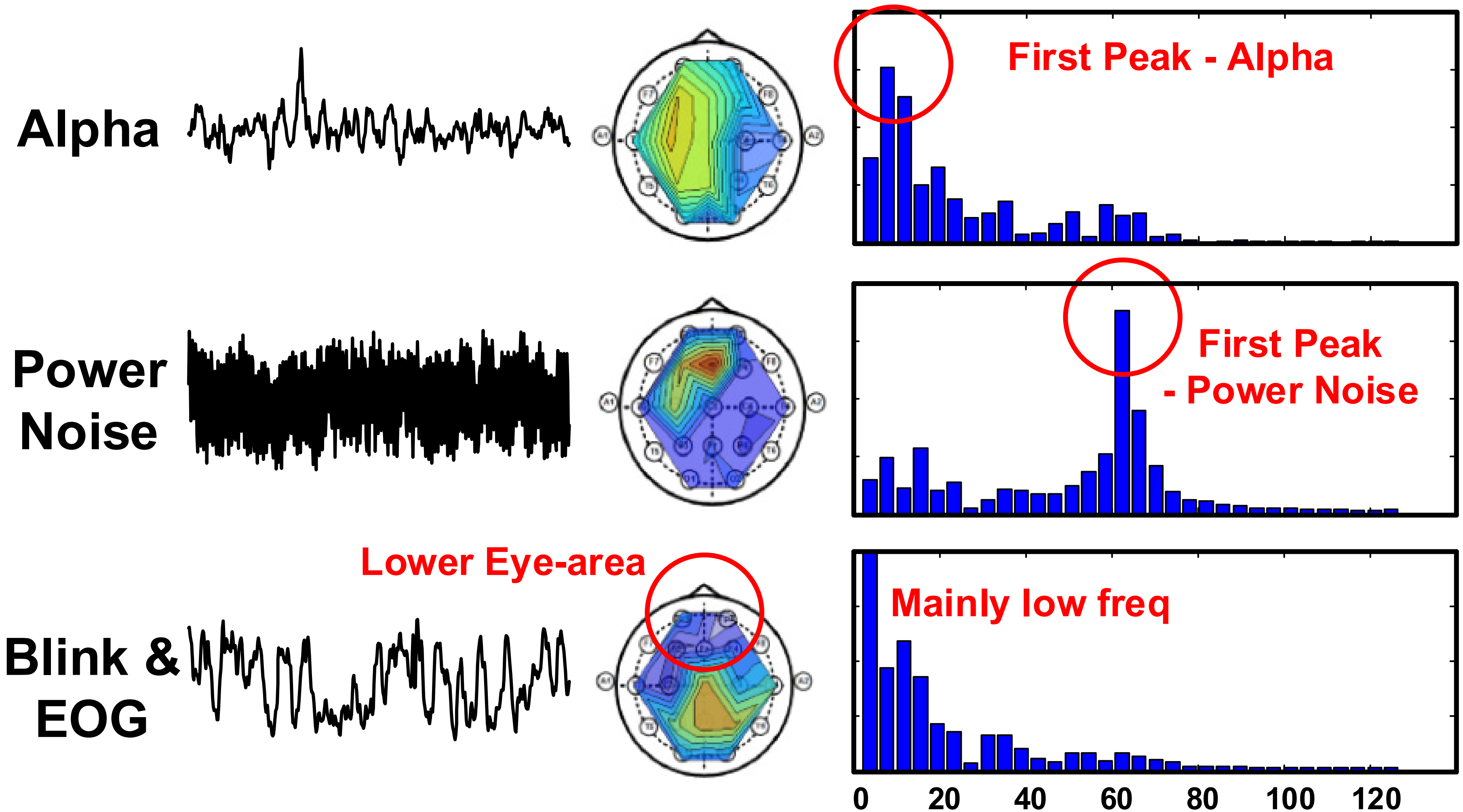


Database for Source Selection

- Power spectrum (1st / 2nd peak freq.)
- Activation locations of selected sources

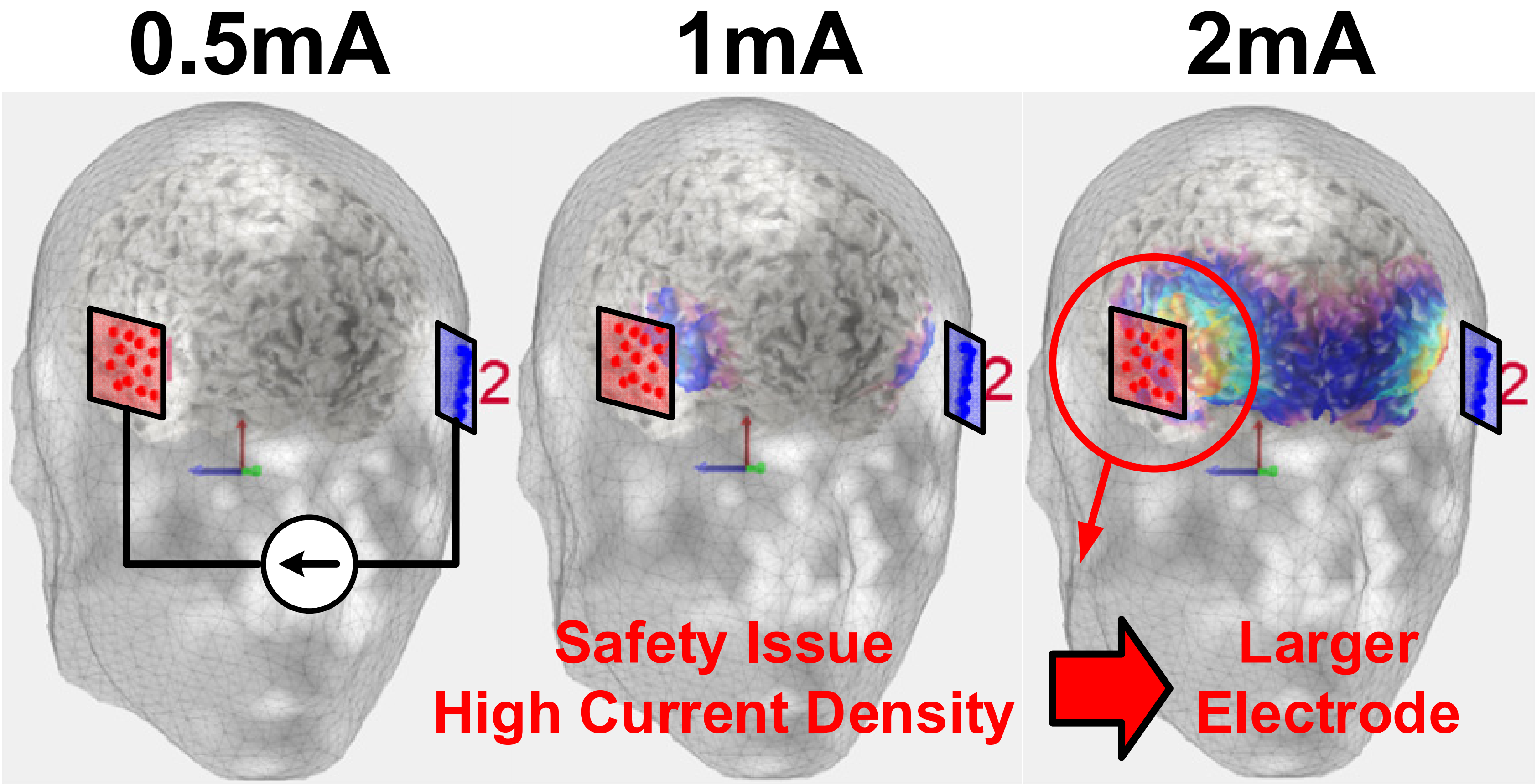


Measurement of Monitoring



Stimulation Analysis vs. Current

- Frontal Stimulation (20x20mm^2 electrodes)
  - Safety Issue : Current Density < 60uA/cm2

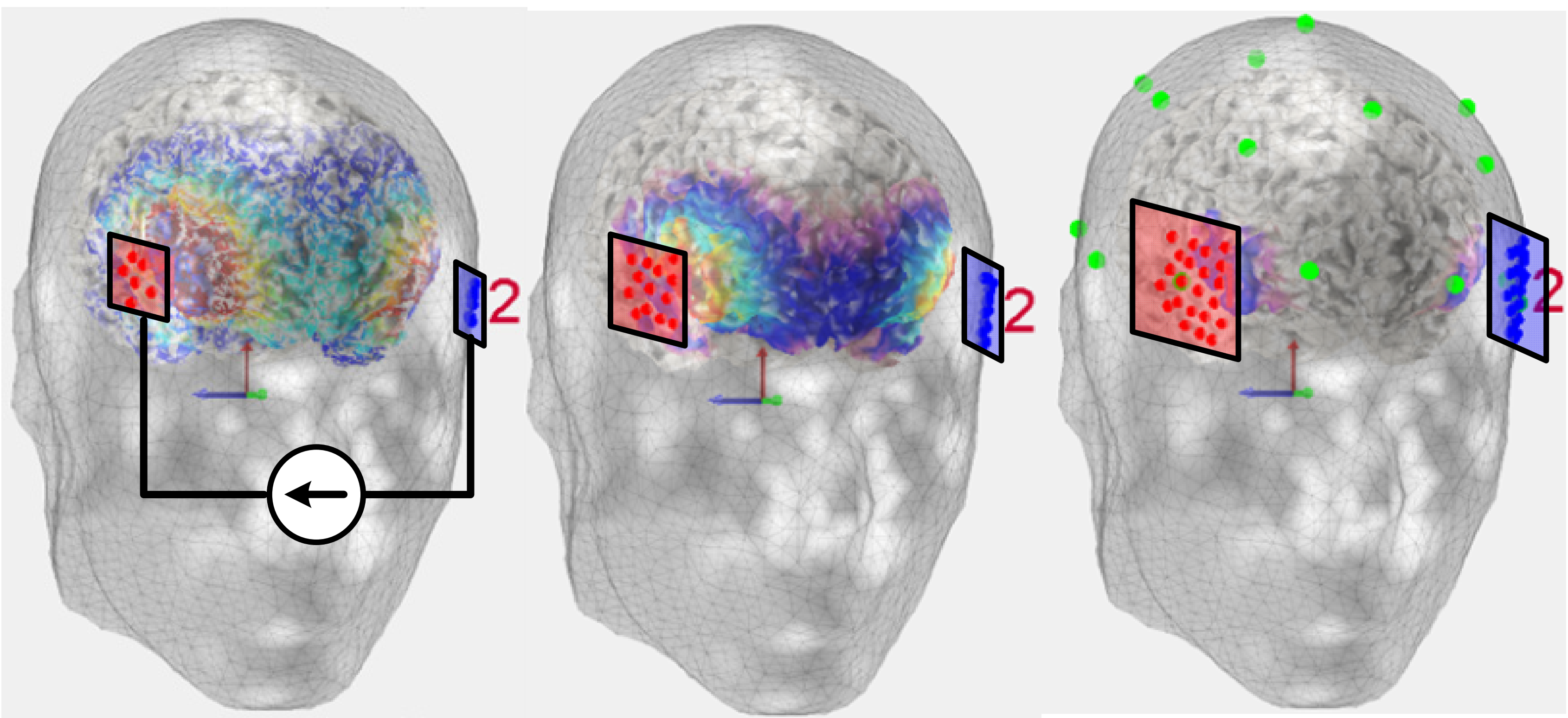


Stimulation Analysis vs. Elec. Size

❑Frontal Stimulation (2mA)

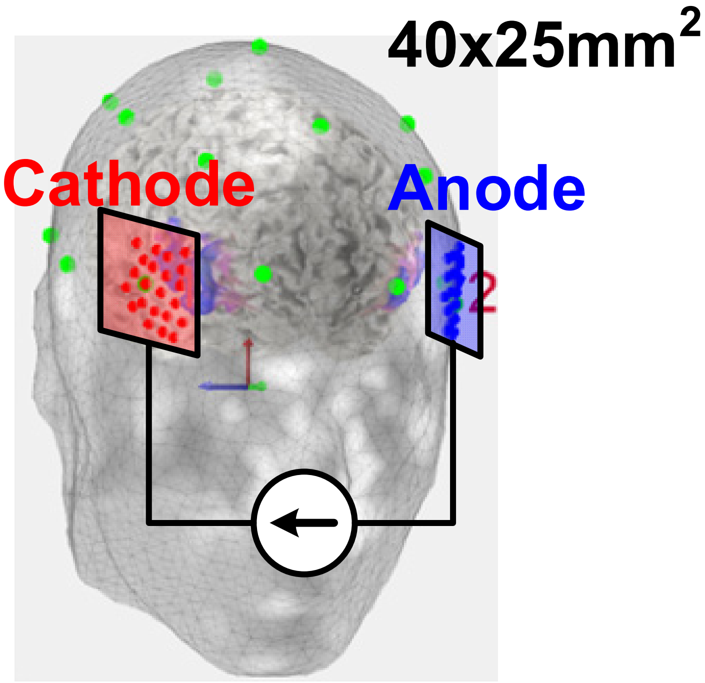
– More than 900mm^2 is required

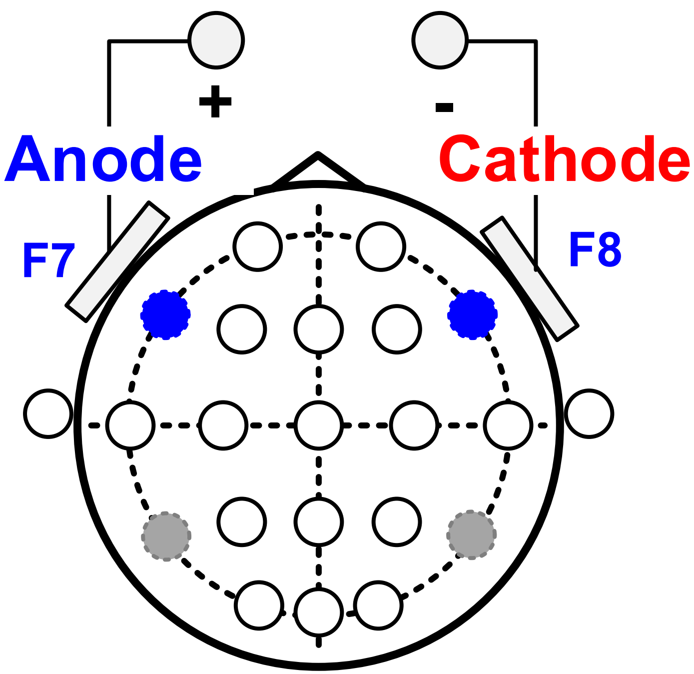
10x10mm^2 20x20mm^2 30x30mm^2



Electrode Placement for Stimulation

- Electrode Placement for ADHD Therapy
- 40x25mm^2 electrodes in F7 and F8 position
  - The frontal lobe is affected.

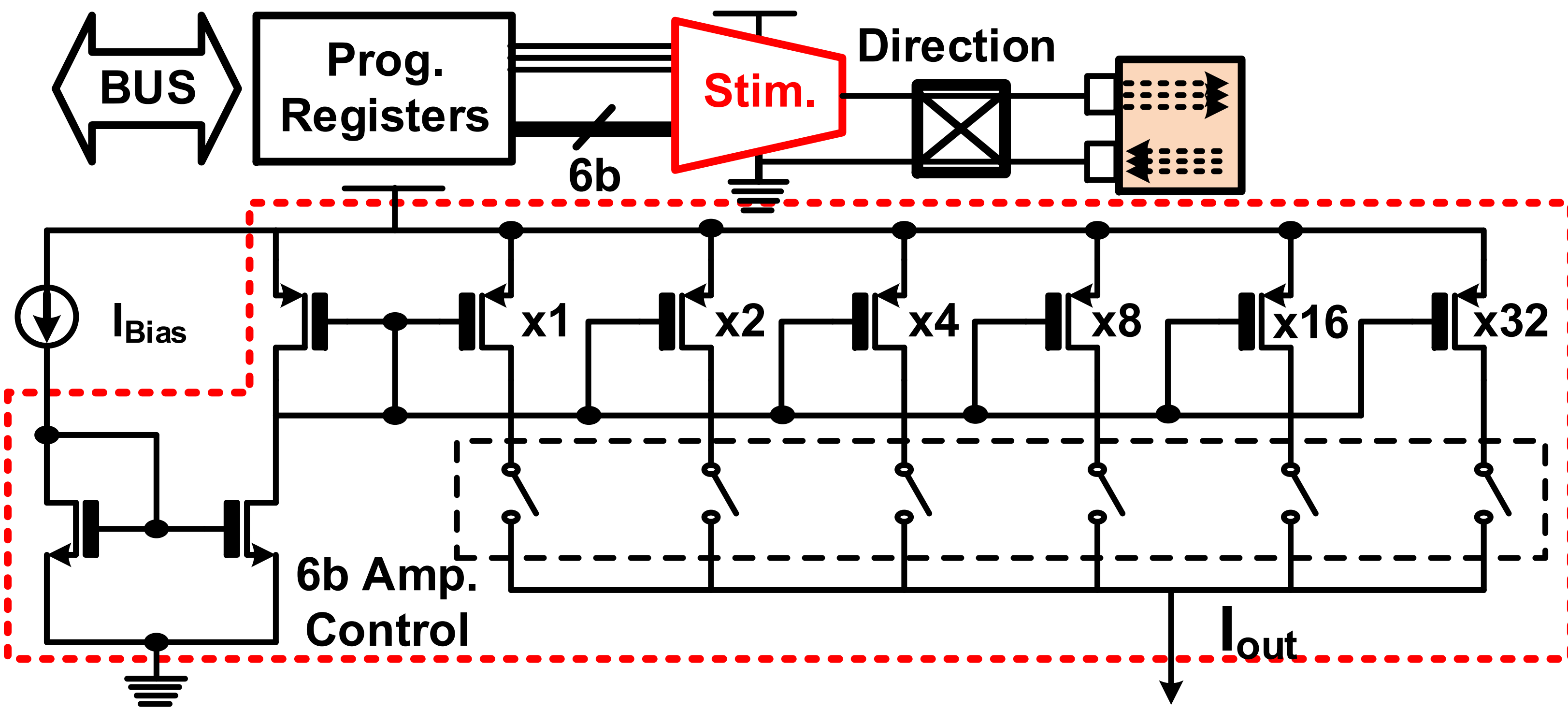




6b Current Steering DAC

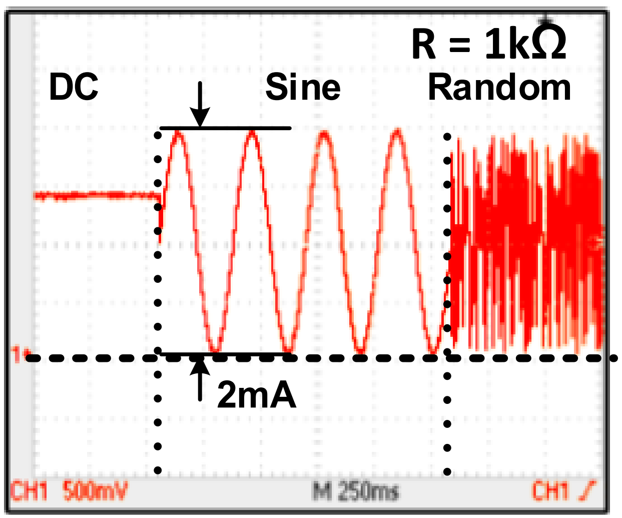
❑Programmable Parameters

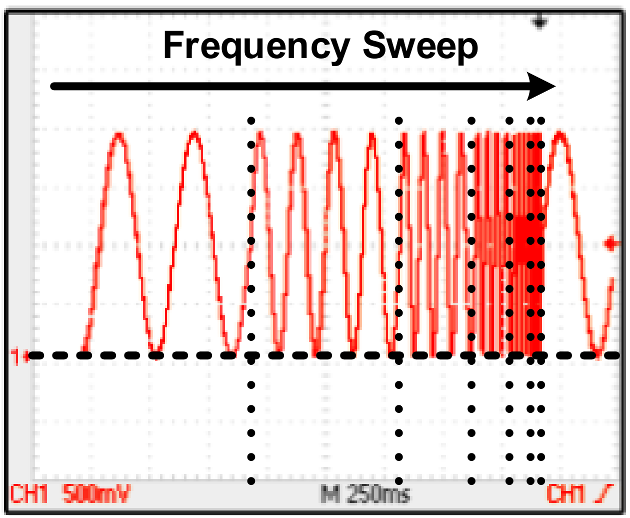
– Current Amplitude, Frequency and Polarity



Stimulation Waveform

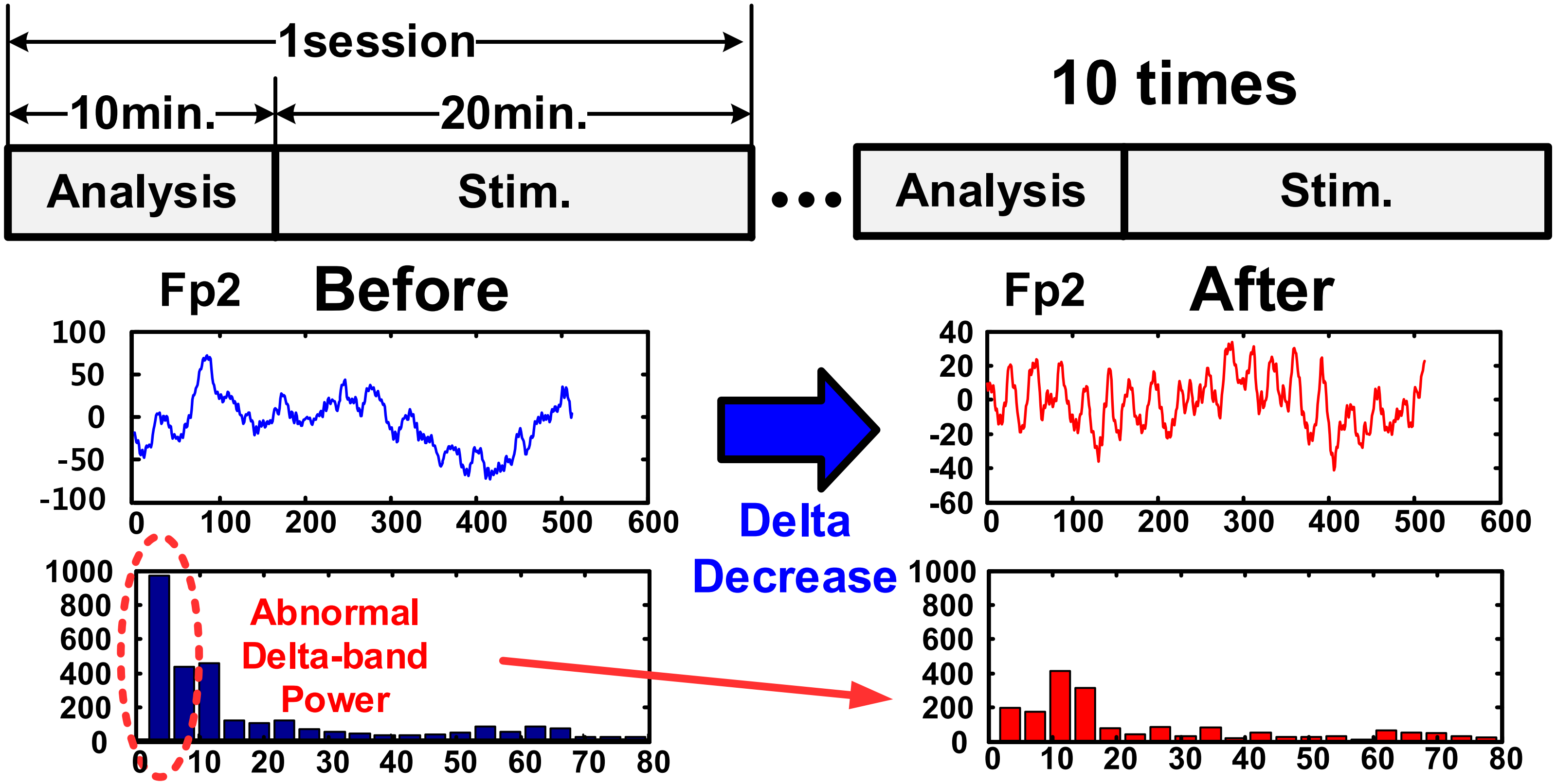
- ❑32µA LSB current up to 2mA
- ❑Various frequency from DC to 1MHz
- ❑Reconfigurable waveform
  - – Direct current, Alternating current, and Arbitrary





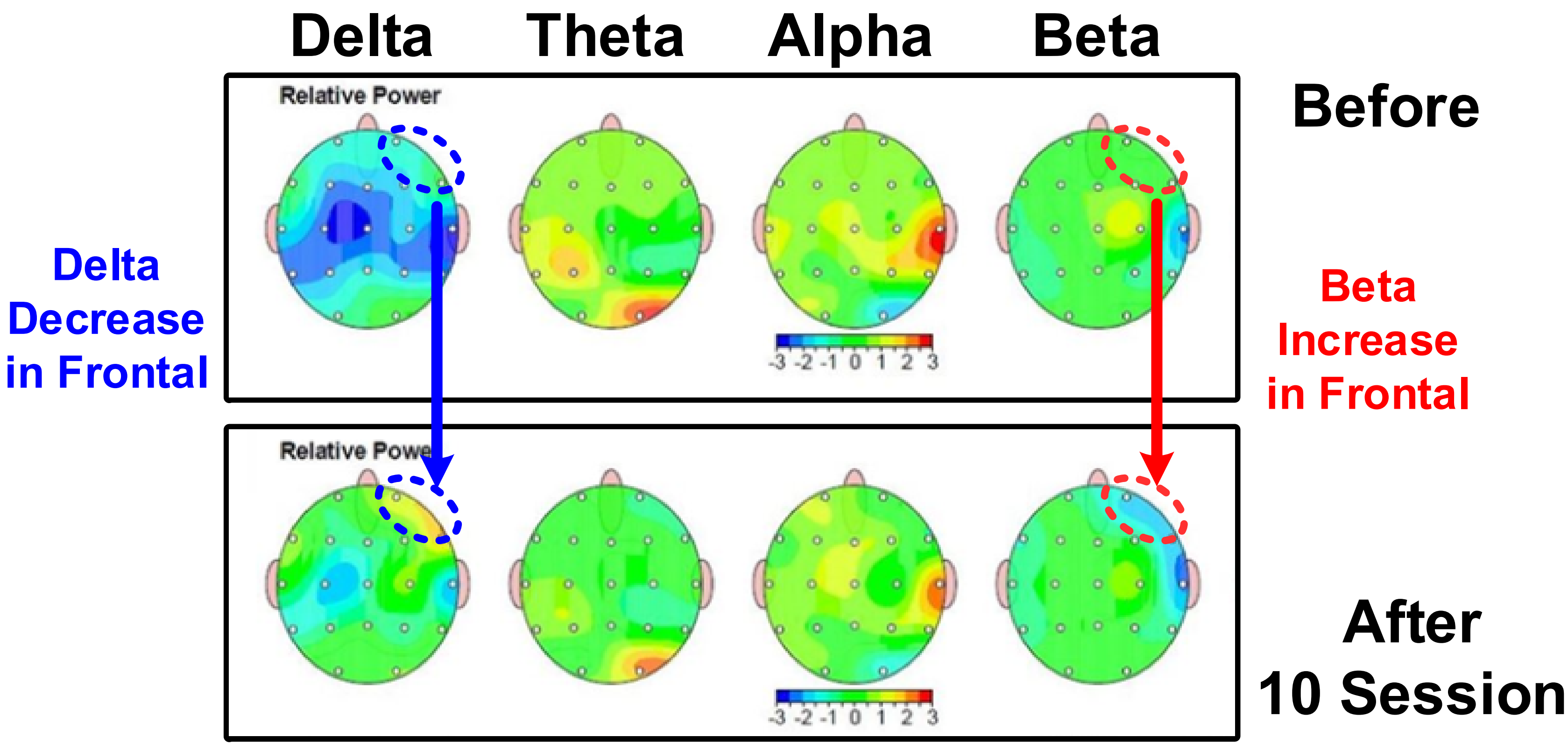
Stimulation Protocol & Results

- ❑ Periodic stimulation protocol
  - ➔ 10-min analysis and 20-min therapy



ADHD(Developmental Lag Pattern)

- 2mA tDCS, bifrontal (Right Anode)
- 10 sessions (20min stim.)

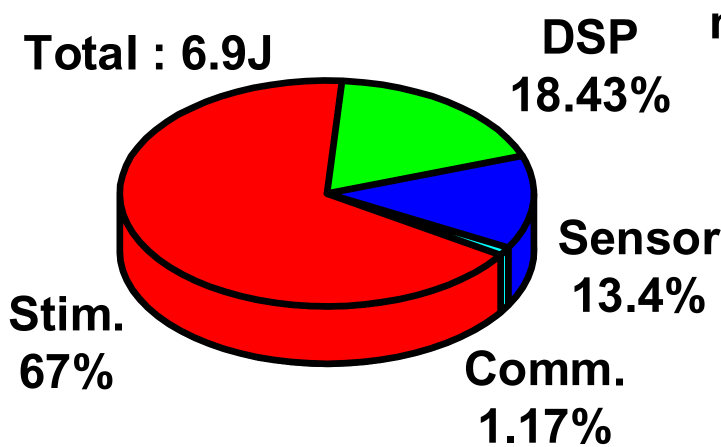


Measurement Results

- 6.9J/Session (Avg. 3.83mW)
- Different power modes vs. # of IC

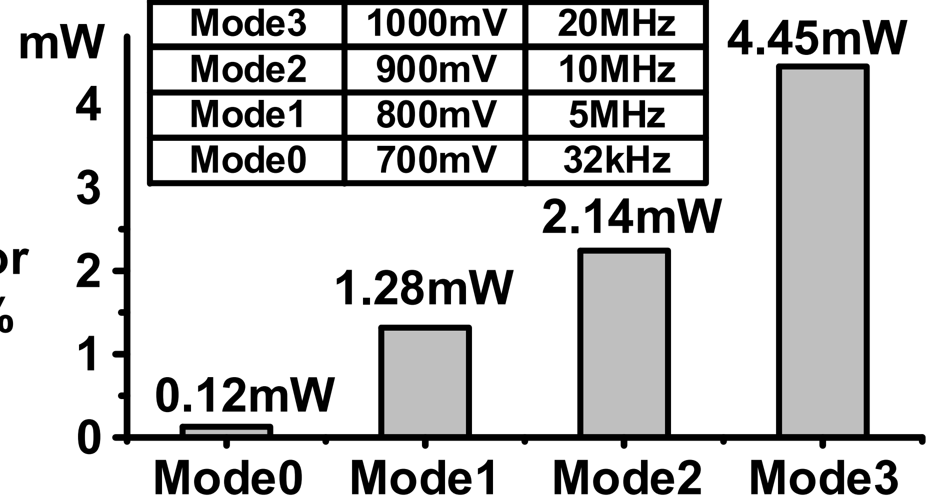
Energy break-down (1session)

20min Stim. & 10min Analysis

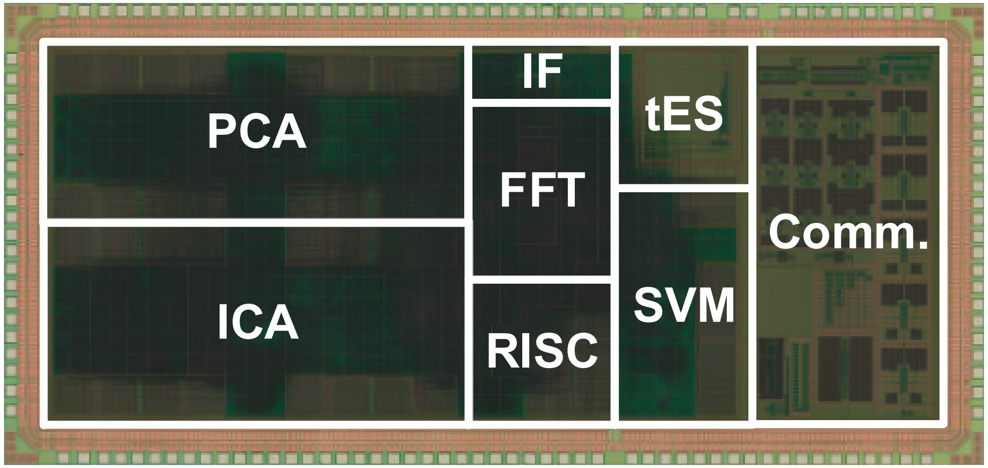


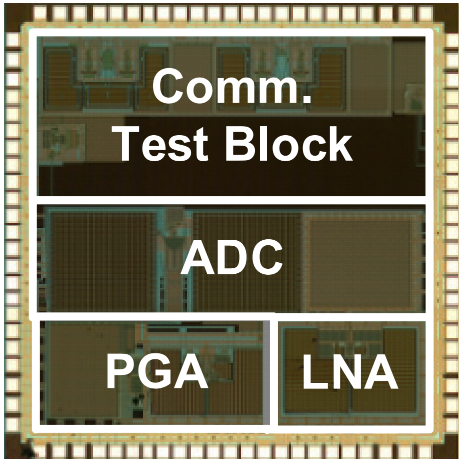
Digital Signal Processor Voltage & Freq. Modes

Mode	Supply	Freq.
Mode3	1000mV	20MHz
Mode2	900mV	10MHz
Mode1	800mV	5MHz
Mode0	700mV	32kHz



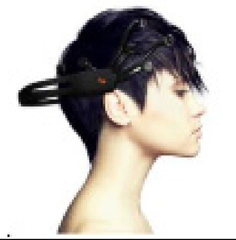
Chip Photograph & Summary





Process		0.13µm CMOS	0.18µm CMOS
Die Size [mm x mm]		2.35 x 5.0	2.35 x 2.35
Supply		0.7-1.0V (core)	1.5V
Power		2.14mW @ 10MHz	75µW
tES	LSB	32µA	-
	Max.	2mA	-
Gain		-	54dB ~74dB
ENOB		-	9.3bit

System Comparison

					
Reference	NeuroSky	Emotiv	ISSCC2012	Soterix	This Work
Sensor Type	Headset	Headgear	Headband	Headset	Headgear
# of Channels	1	14	4	X	16
Application	Entertain	Research	Mental Health	Mental Health	Mental Health
Interface Method	Visual	Visual	Visual	Electrical	Visual & Electrical

Chip Comparison

		ISSCC2012	This Work
Process		0.13µm CMOS	NFS : 0.13µm CMOS AFE : 0.18µm CMOS
Die Size (mm^2)		2.35 x 5.0	NFS : 2.35 x 5.0 AFE : 2.35 x 2.35
Operating Clock Freq.		1MHz	10MHz
Avg. Power	Processor	149µW	2.14mW
	Sensor	77.18µW	75µW
ICA	# of Channels	4	16
	Method	FastICA	FastICA
Classification		-	Linear Support Vector Machine
FoM(W/Ch^2)		9.31µW/Ch^2	8.32µW/Ch^2

Conclusion

- Neuro-feedback Headgear System
  - 16 analog front-end IC
  - Neuro-feedback SoC w/ monitoring and therapy
- Mental Health Monitoring (Processor)
  - 91% of independent component selection
  - 2.14mW average power consumption
- Brain Stimulation Therapies (PES)
  - Up to 2mA programmable parameter
  - tES : DC-1MHz Arbitrary waveforms

2.5D Heterogeneously Integrated Bio-Sensing Microsystem for Multi-Channel Neural Sensing Applications

P.-T. Huang, L.-C. Chou, T.-C. Huang, S.-L. Wu, T.-S. Wang, Y.-R. Lin, C.-A. Cheng, W.-W. Shen, K.-N. Chen, J.-C. Chiou, C.-T. Chuang, W. Hwang, K.-H. Chen, C.-T. Chiu, M.-H. Cheng, Y.-L. Lin and H.-M. Tong

National Chiao Tung University
China Medical University
Advanced Semiconductor Engineering (ASE) Group

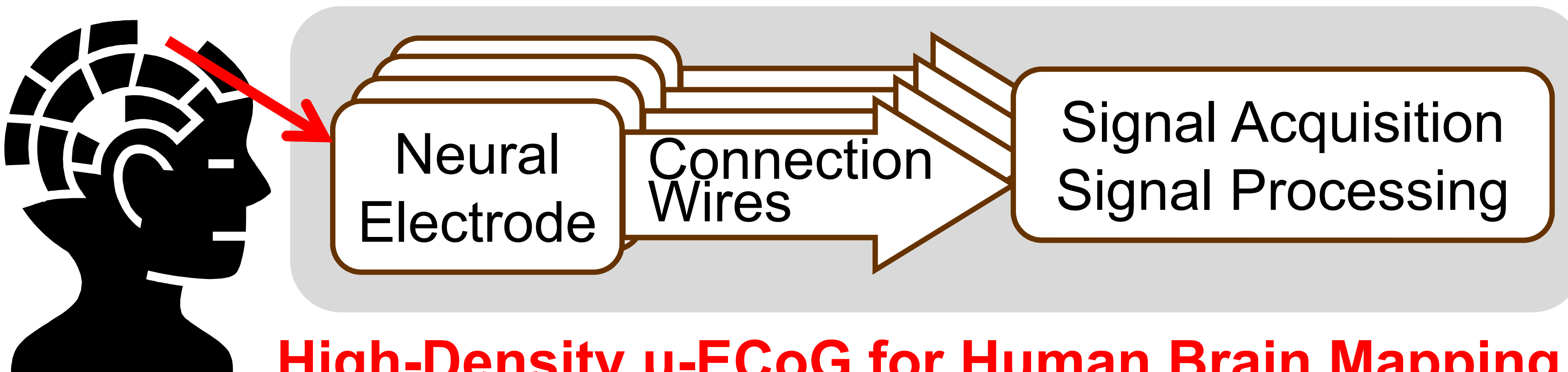
Outline

- Introduction
- 2.5D integrated bio-sensing microsystem
  - System architecture
  - 2.5D heterogeneous integration
- Key components for 2.5D bio-sensing microsystem
  - TSV-inside μ-probe array
  - Multi-channel neural signal acquisition
  - Configurable Discrete Wavelet Transform (DWT)
  - On-interposer bus
- Fabrication and experimental results
- Conclusions

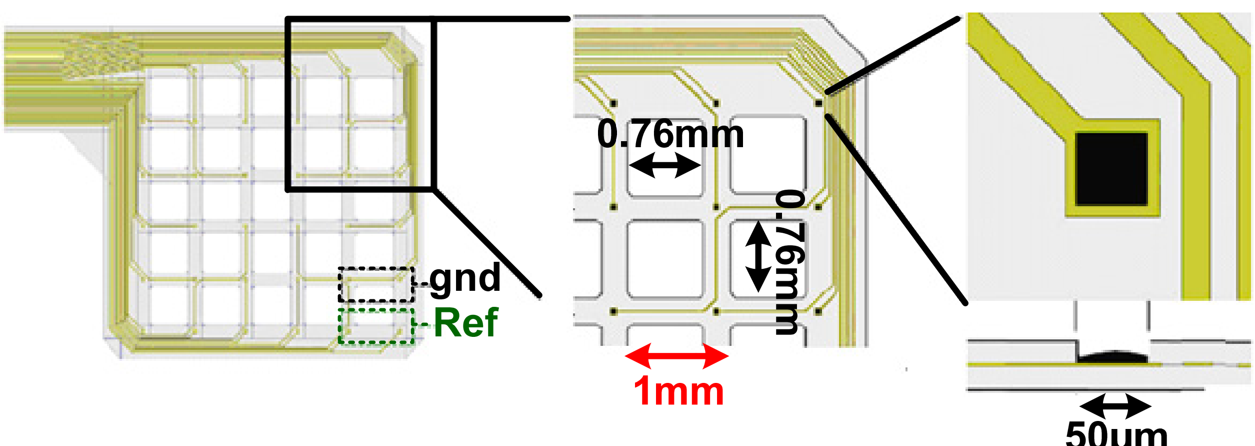
High-Density μ-ECoG Sensing

- Integrated microsystems for neural sensing (μ-ECoG) provides observation on brain activities from subject in natural habitat.

ECoG: Electrocorticography



High-Density μ-ECoG for Human Brain Mapping

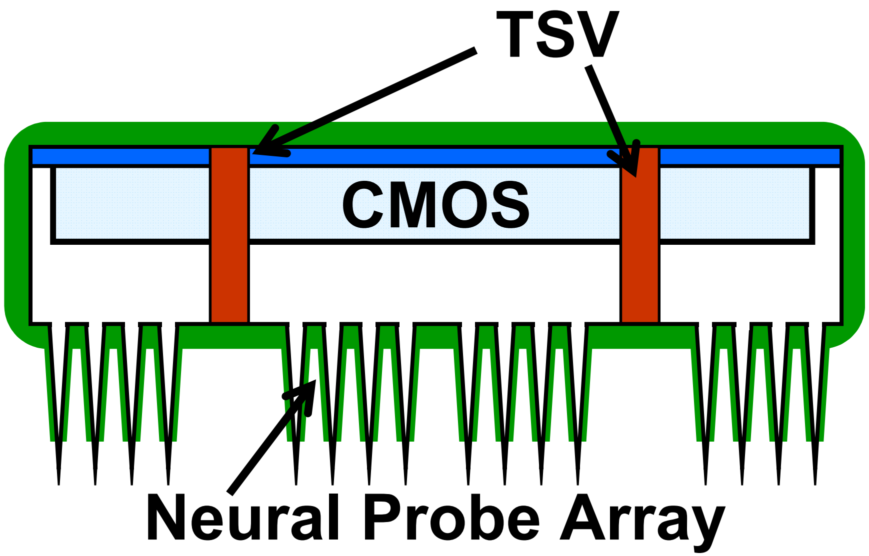


Size	50×50(um^2)
Pitch	1(mm)

[Toda H., 2011]

Double-Side Integration in ISSCC'13

- CMOS and neural probes on two sides of a single chip
- TSVs serve as interconnection inside the chip
- Achieve small-form-factor, shrink in planar and vertical dimensions compared with other multi-chip solutions



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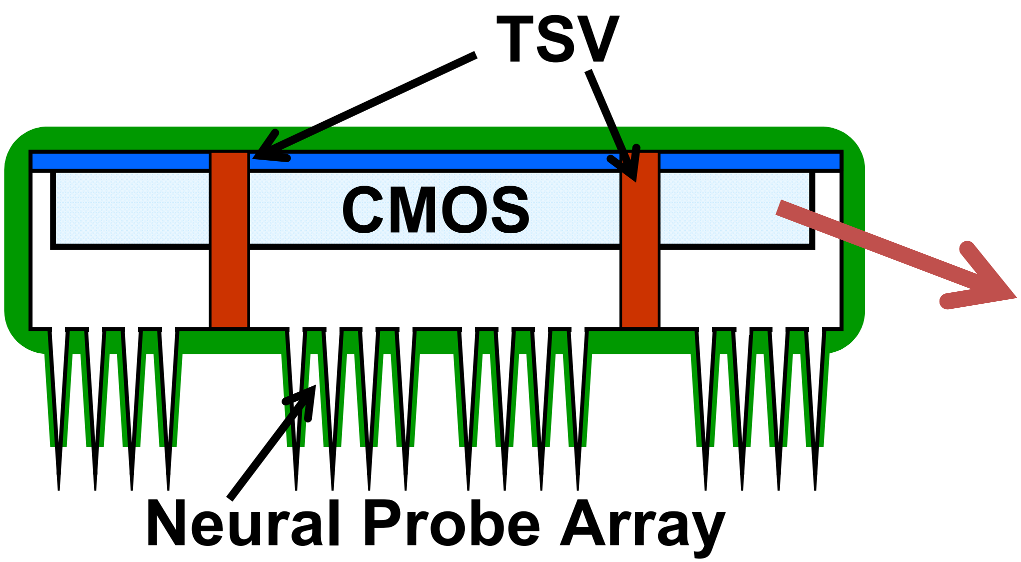
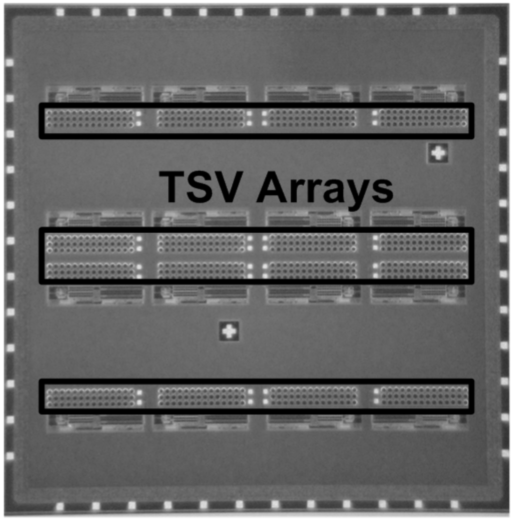
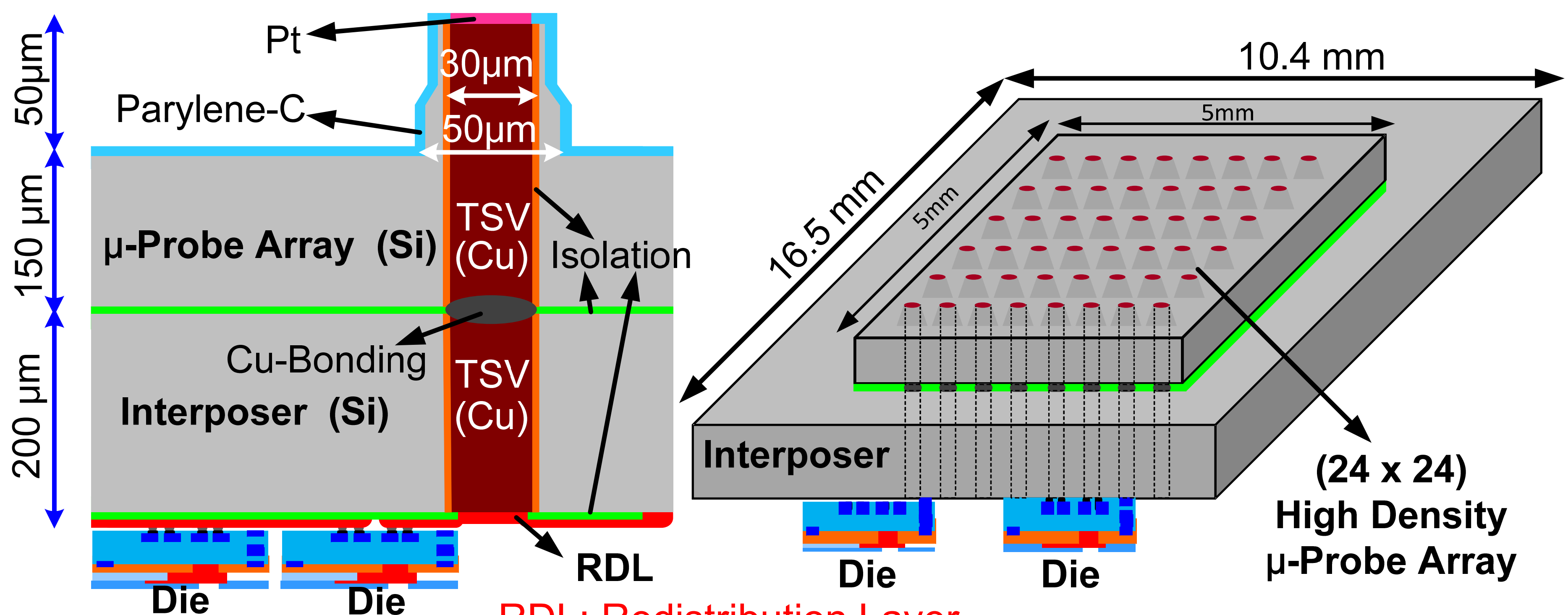




- ◆ **Large area for TSV arrays**
- ◆ **Potential damage on CMOS circuits due to TSV fabrication**

2.5D Integrated Microsystem

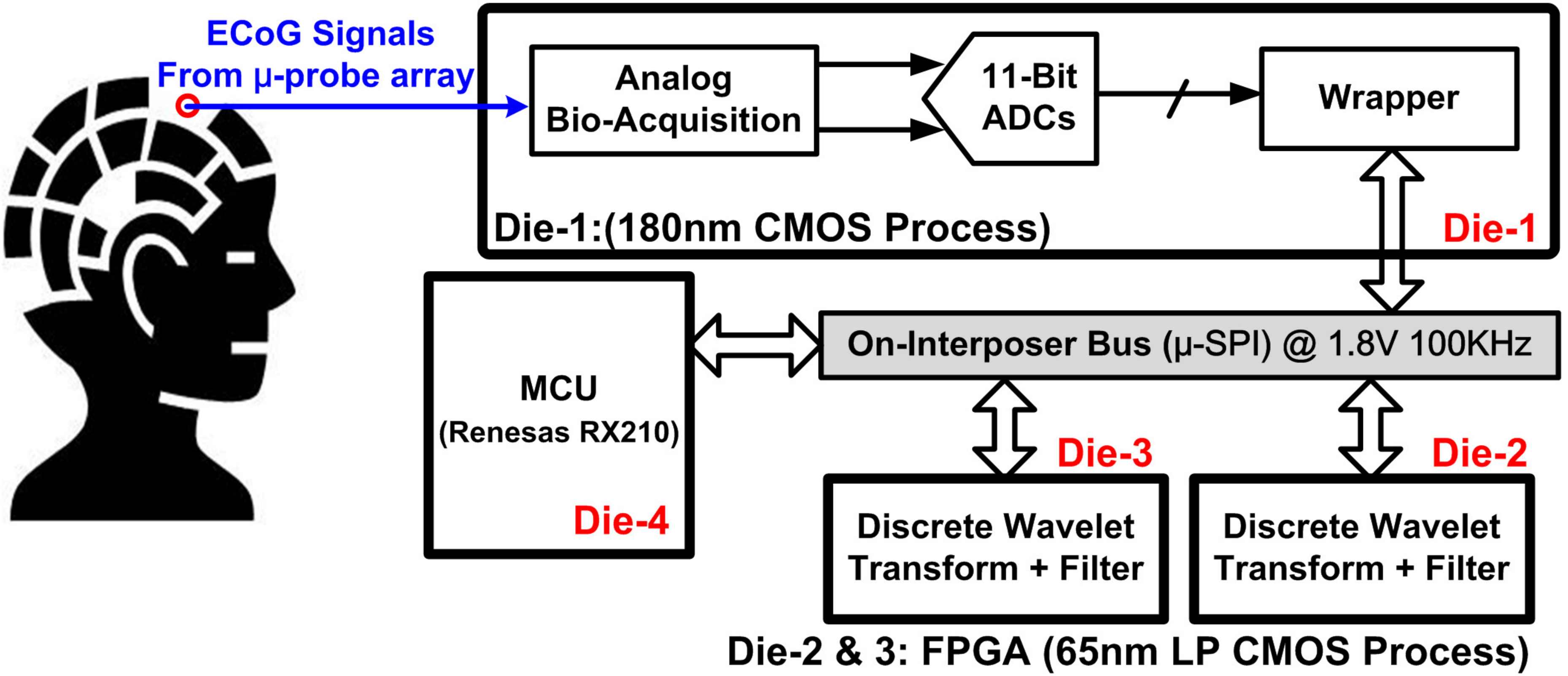
- Supporting platform: silicon interposer
- 24x24 TSV-inside μ-probe array
- Multi-chip solution



RDL: Redistribution Layer

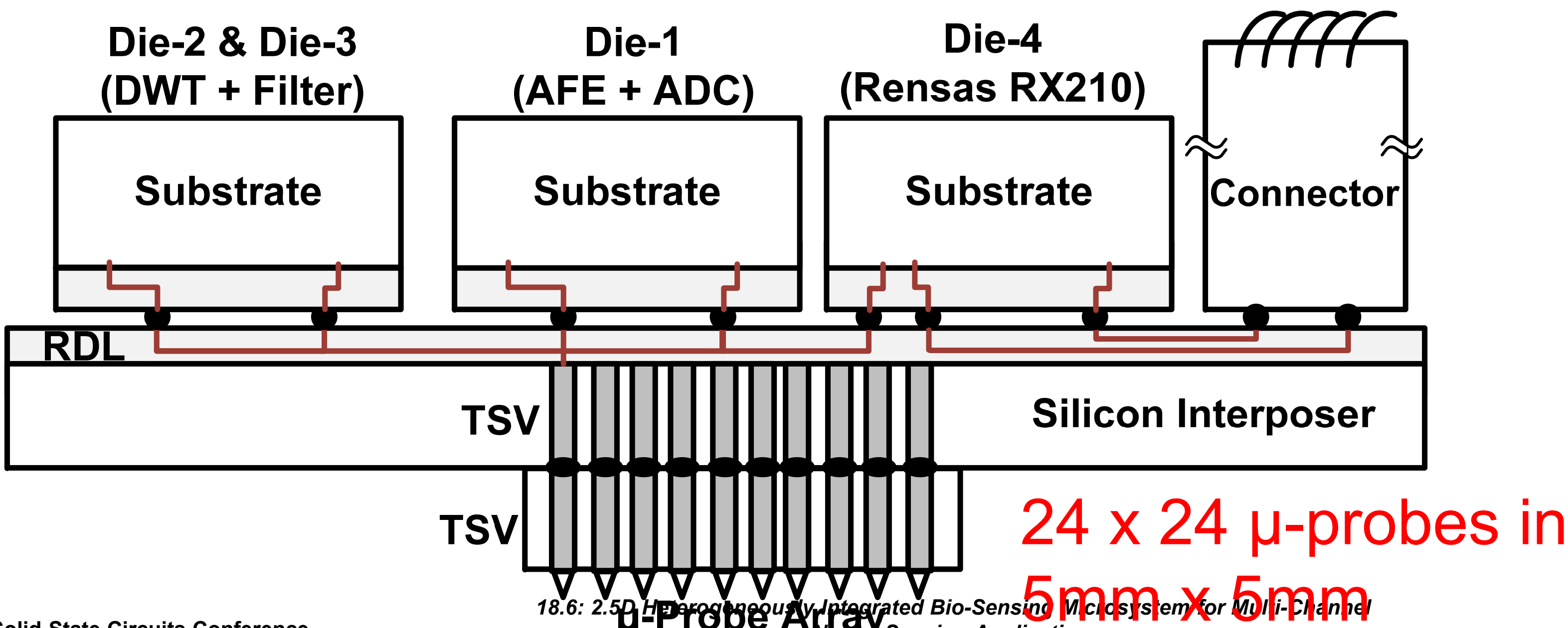
Heterogeneous Multi-Chip Solution

- 2.5D heterogeneous platform
  - 4 dies with different technologies
  - Bare dies: Die-2, Die-3, Die-4



Cross-Section of 2.5D Integration

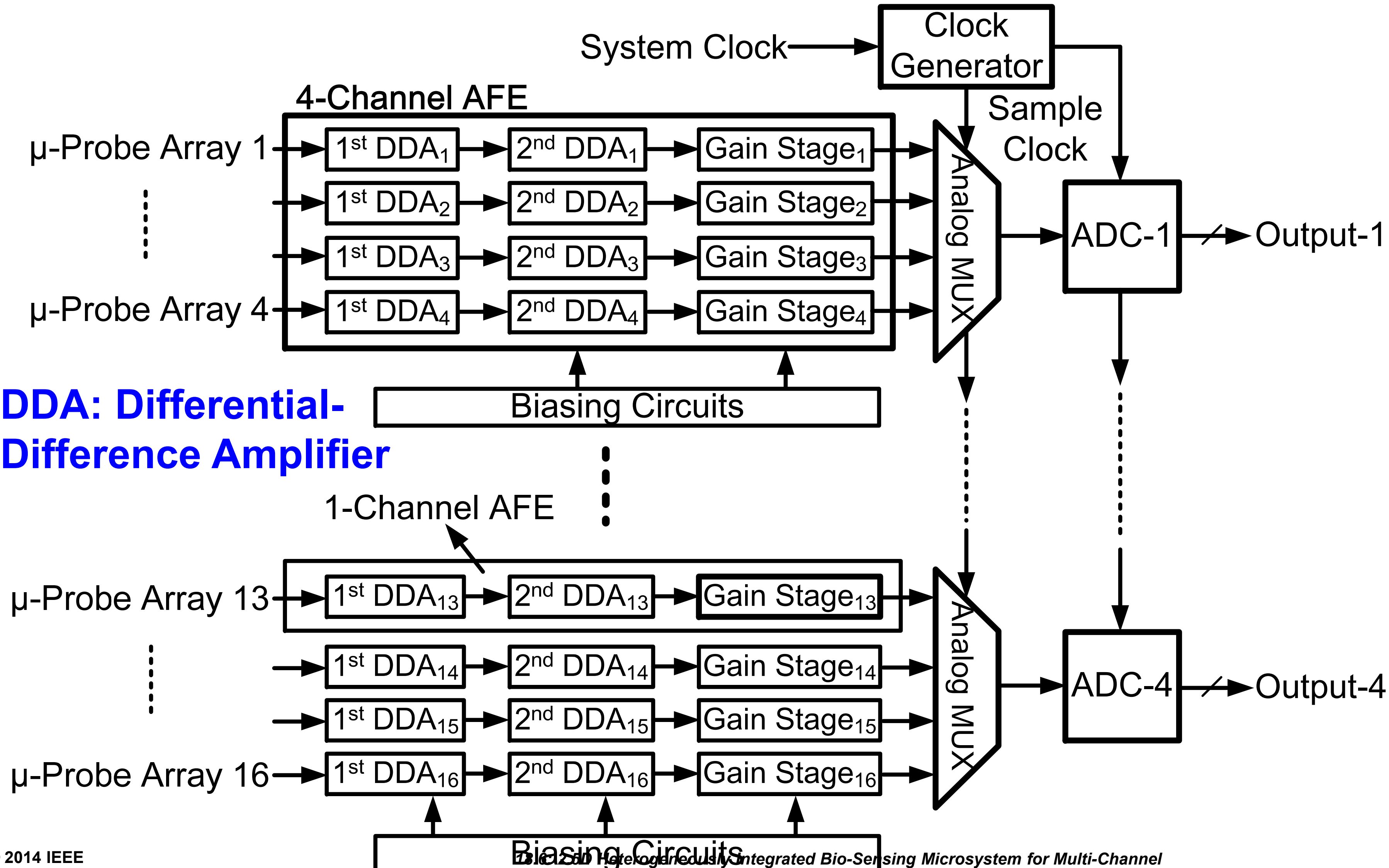
- 2-layer Redistribution Layer (RDL)
  - – Interconnection of interposer
- Configurable sensing channel
  - Each μ-probe connected to 2 cascode TSVs
  - Defined by the connection of RDL
  - 16-channel ECoG in 5mm x 5mm, 36 μ-probes/CH



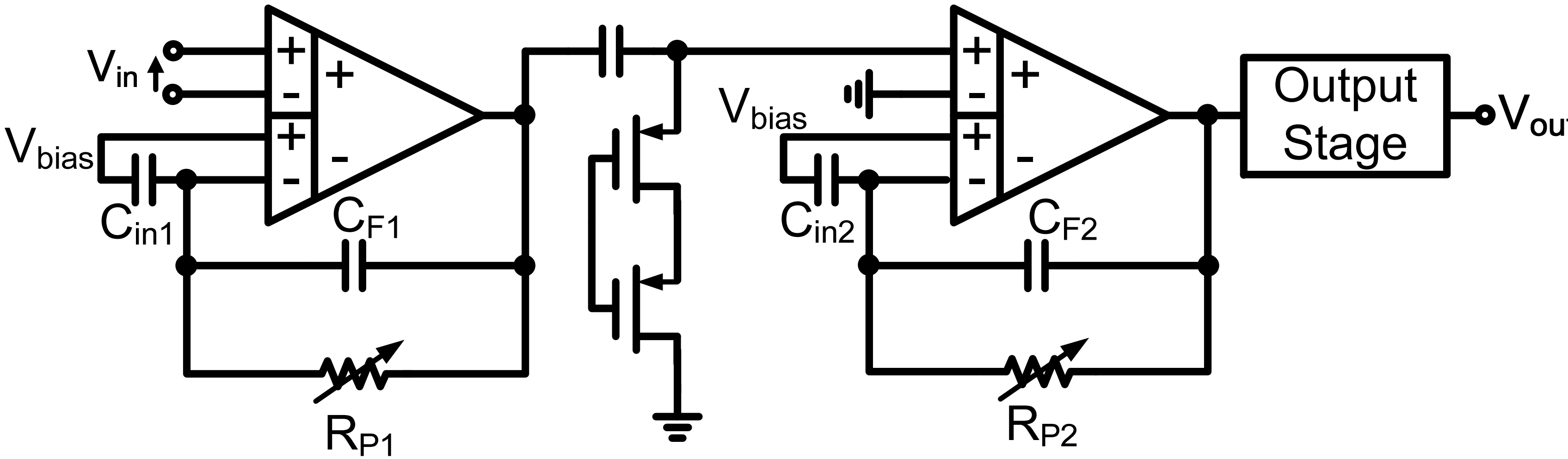
16-Channel ECoG Acquisitions

AFE: Analog Front-End **ADC: Analog-to-Digital Converter**

DDA: Differential-Difference Amplifier

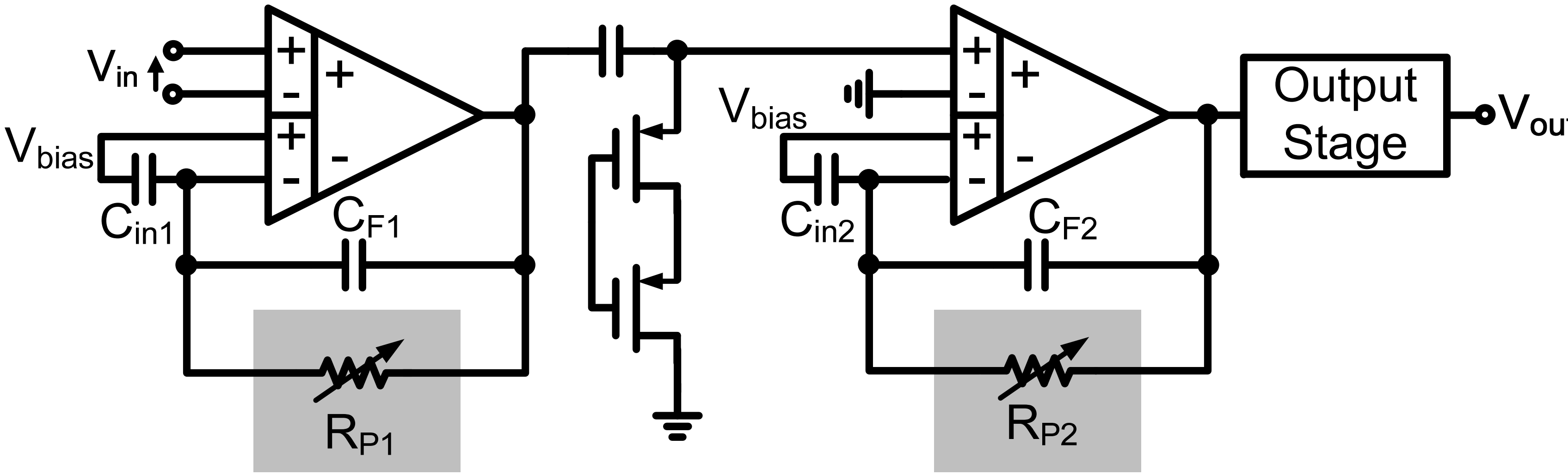


1-Channel AFE Circuitry

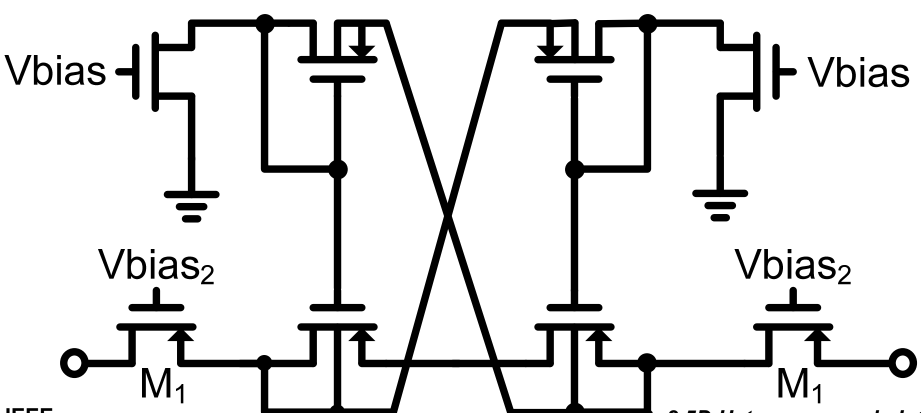


- 2 DDA stages + 1 output stage

1-Channel AFE Circuitry

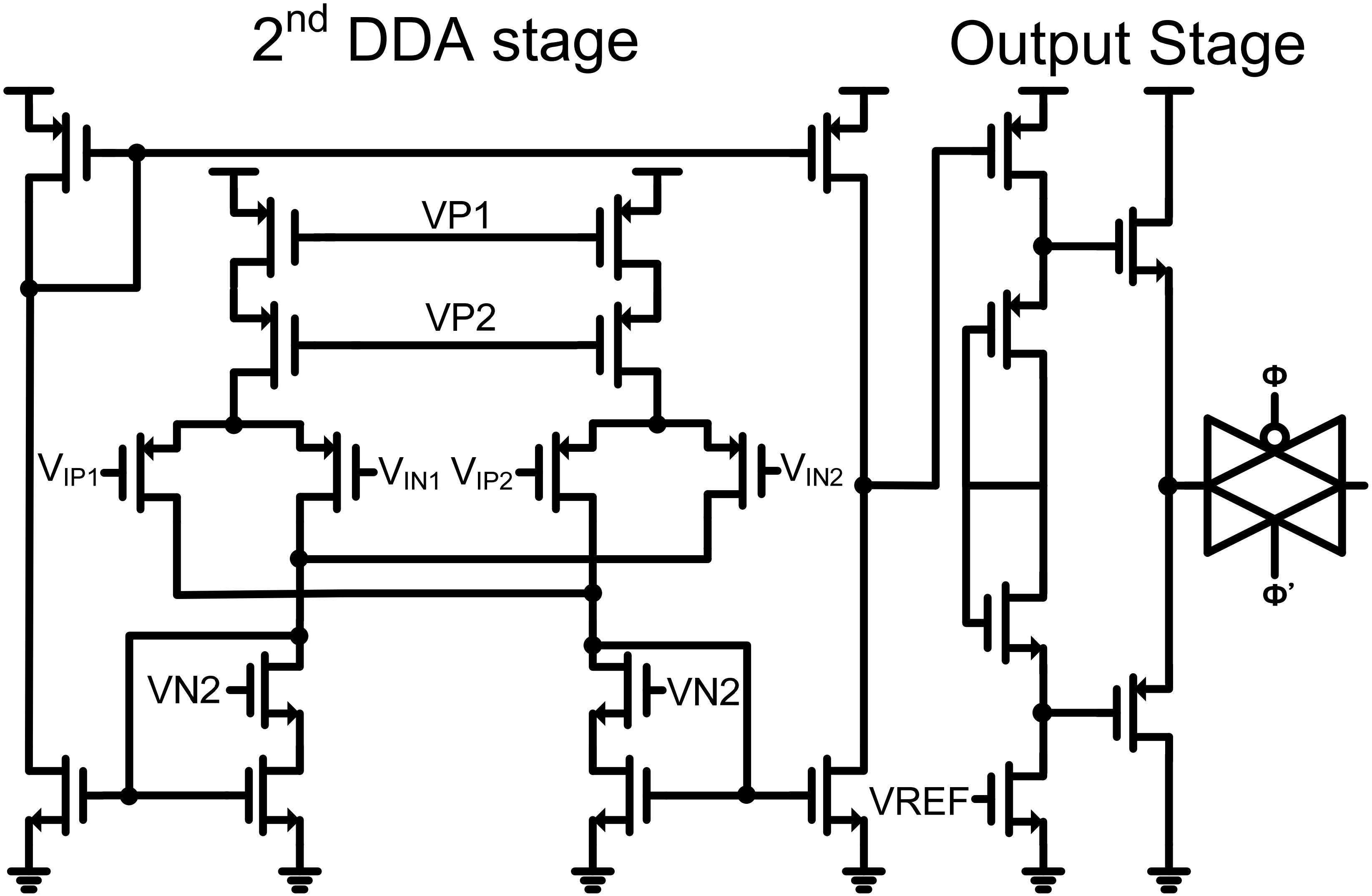


- 2 DDA stages + 1 output stage
- Pseudo resistor for DC offset cancellation

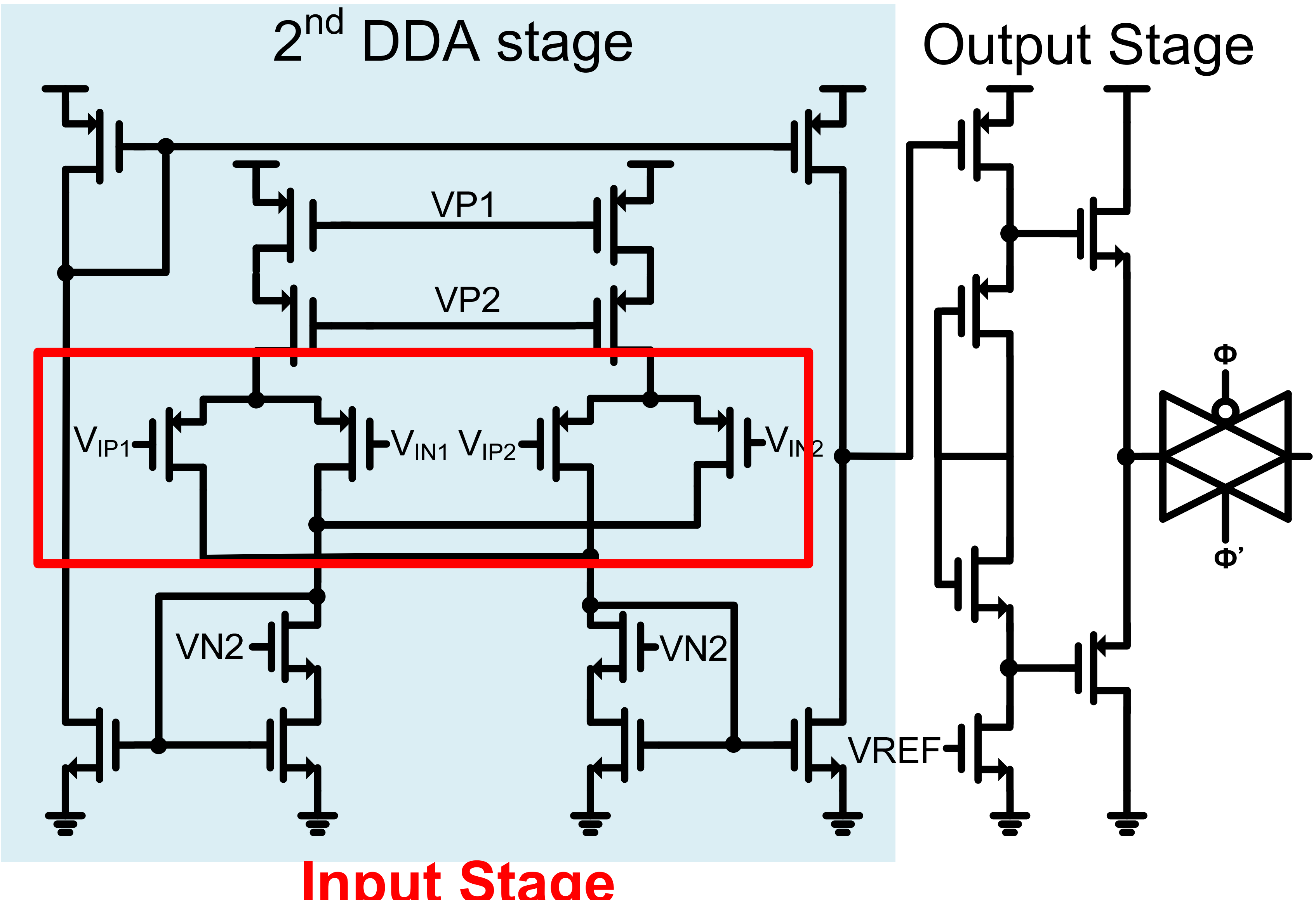


Large resistance for small f_{3db} of high pass filter

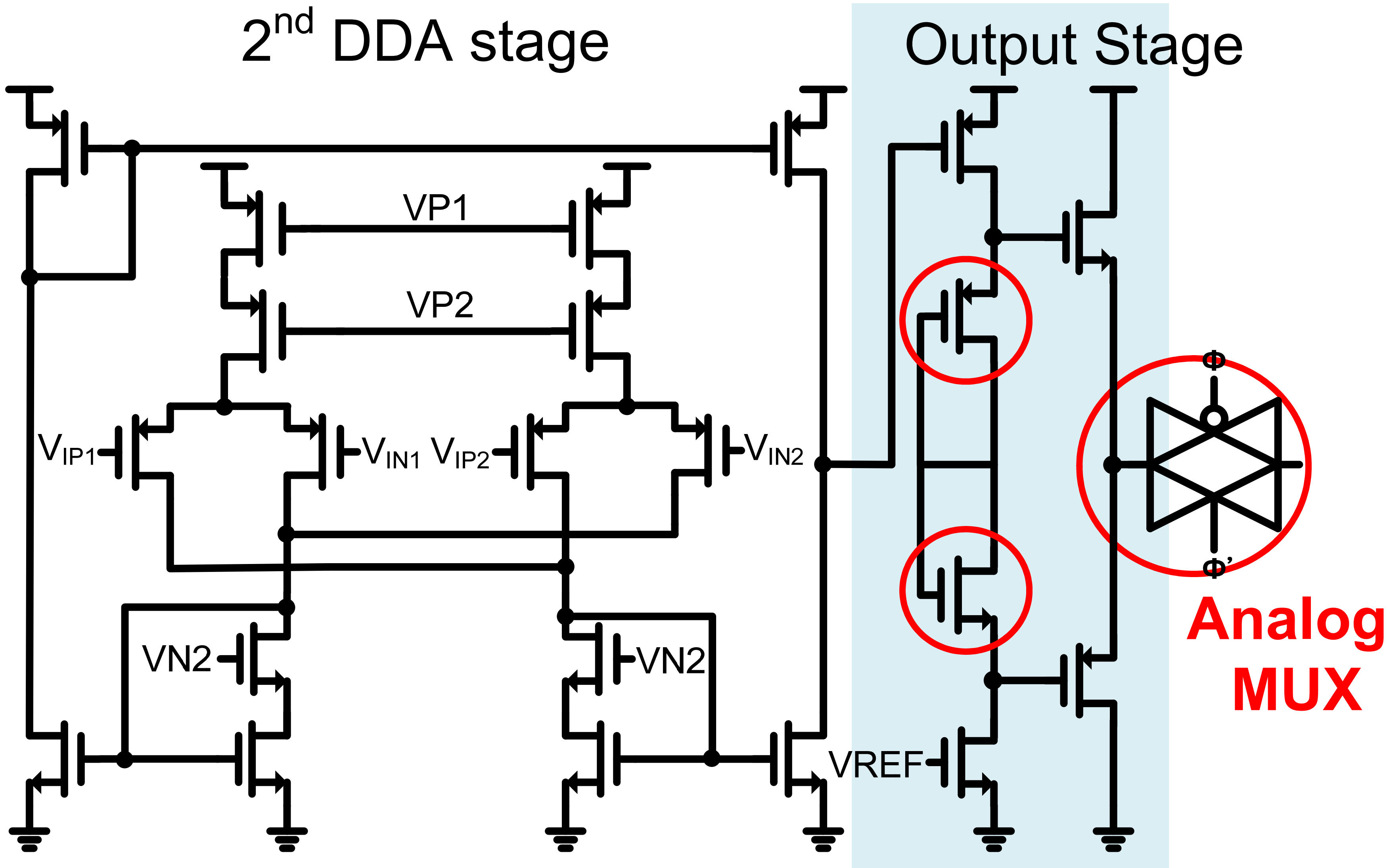
DDA + Output Stage



DDA + Output Stage

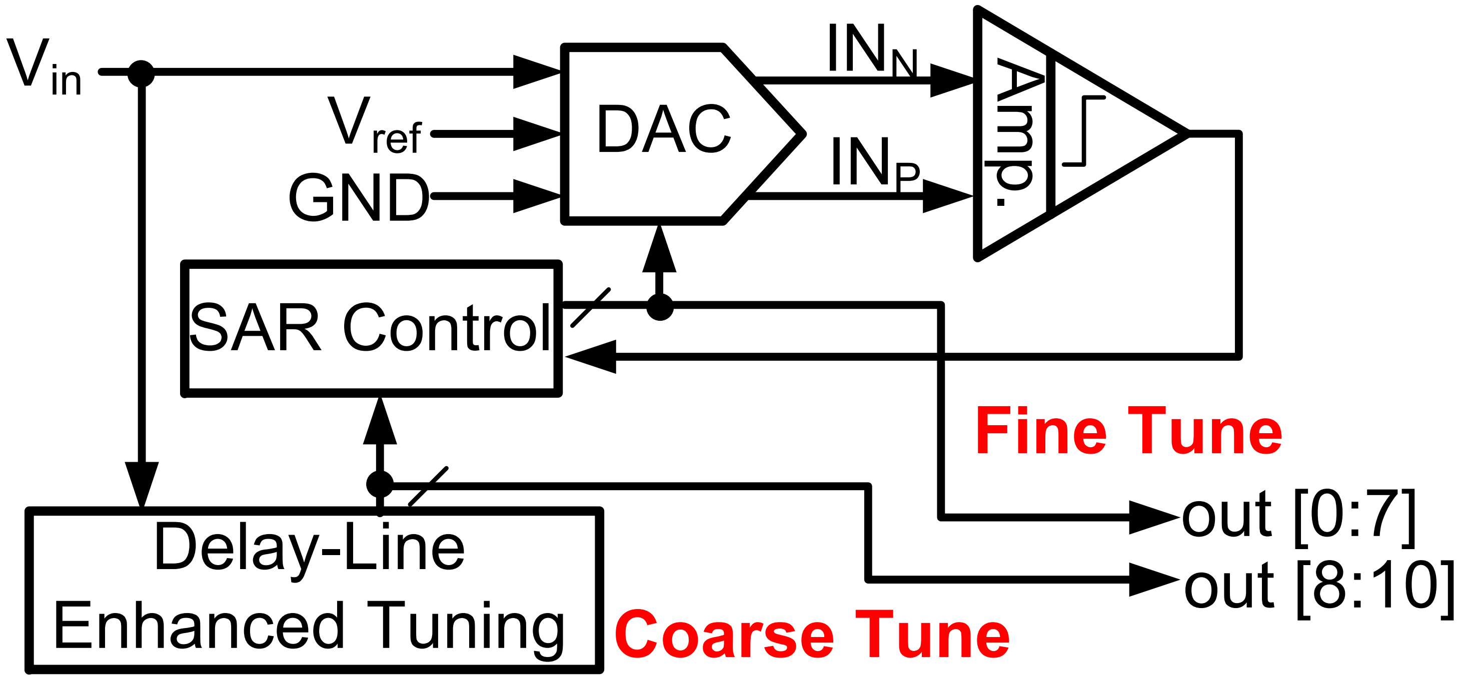


DDA + Output Stage



Area-Power-Efficient 11-Bit ADC

- 8-bit fine-tuning SAR ADC for precise conversion
- 3-bit delay-line enhanced tuning block
  - Reduce the total size of capacitor array in SAR ADC
  - Reduce power budget of SAR ADC



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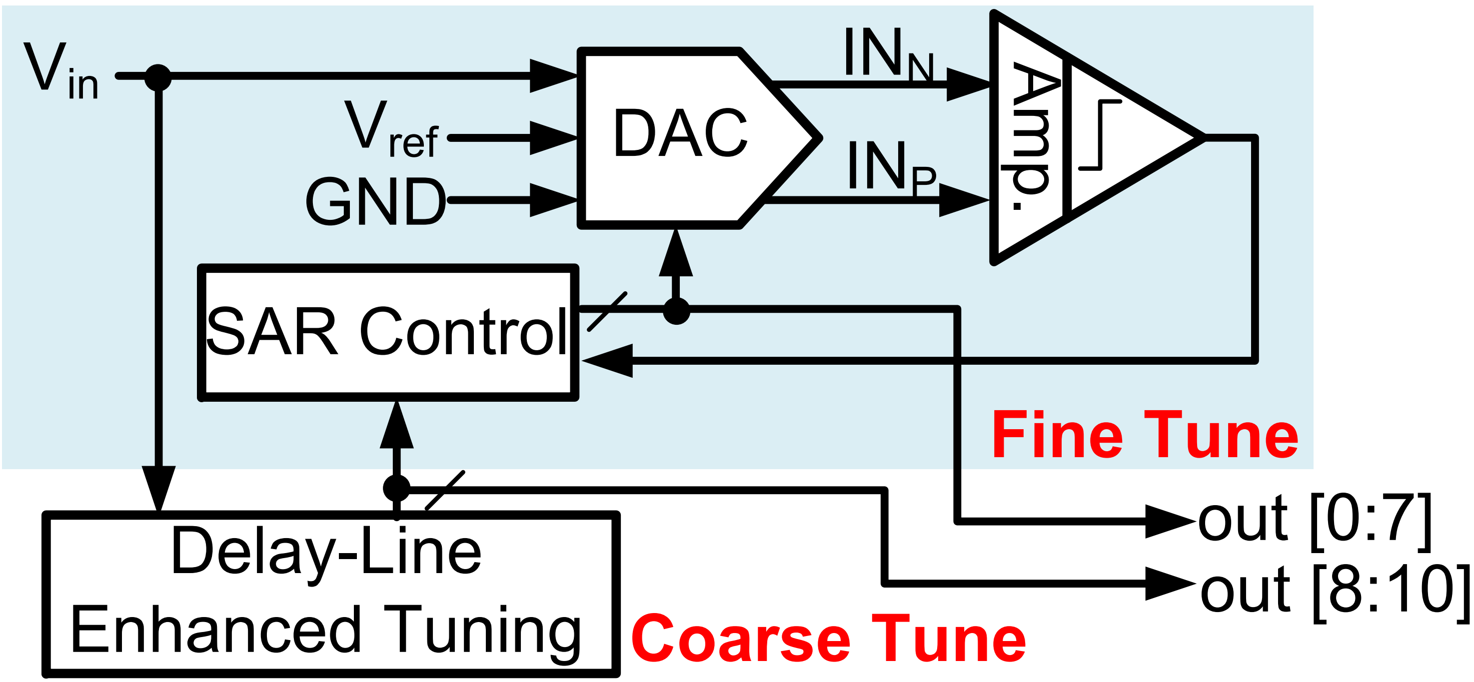
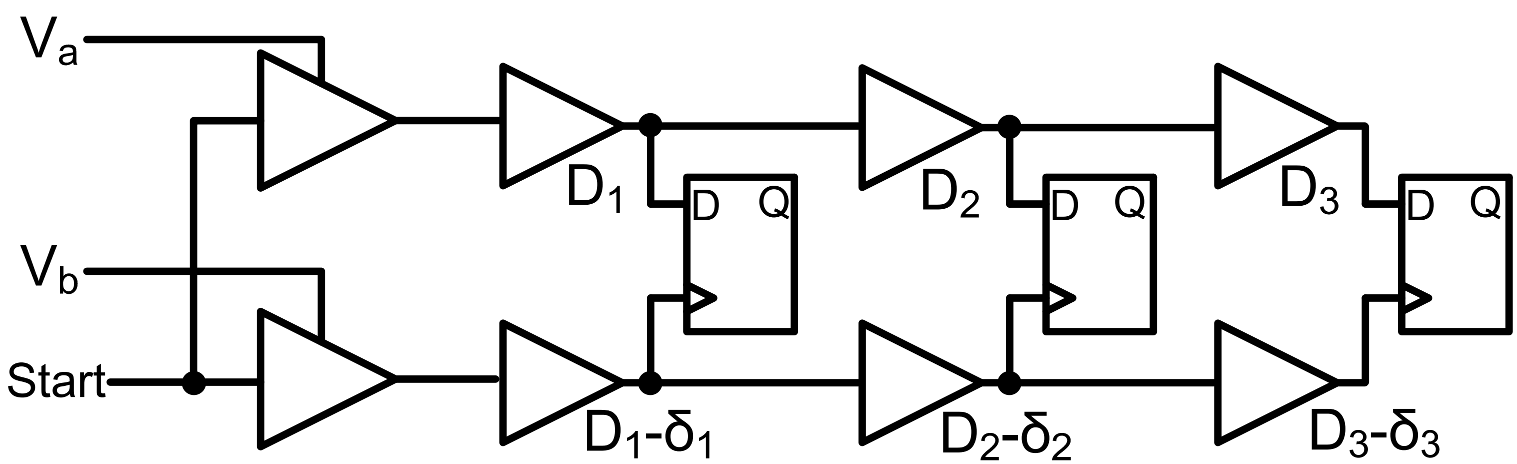
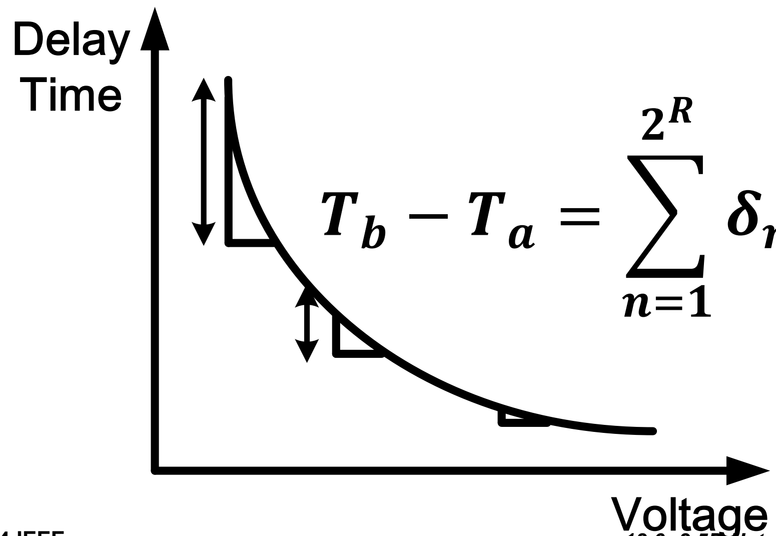


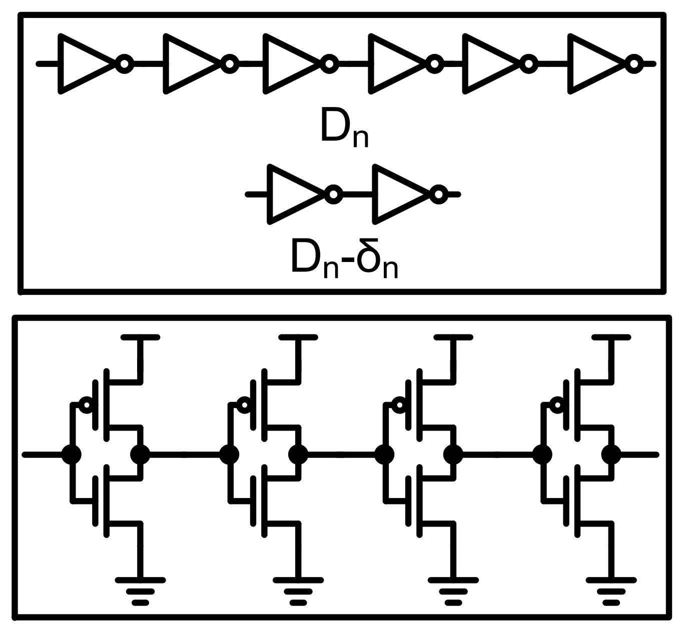
Vernier Time-to-Digital Converter



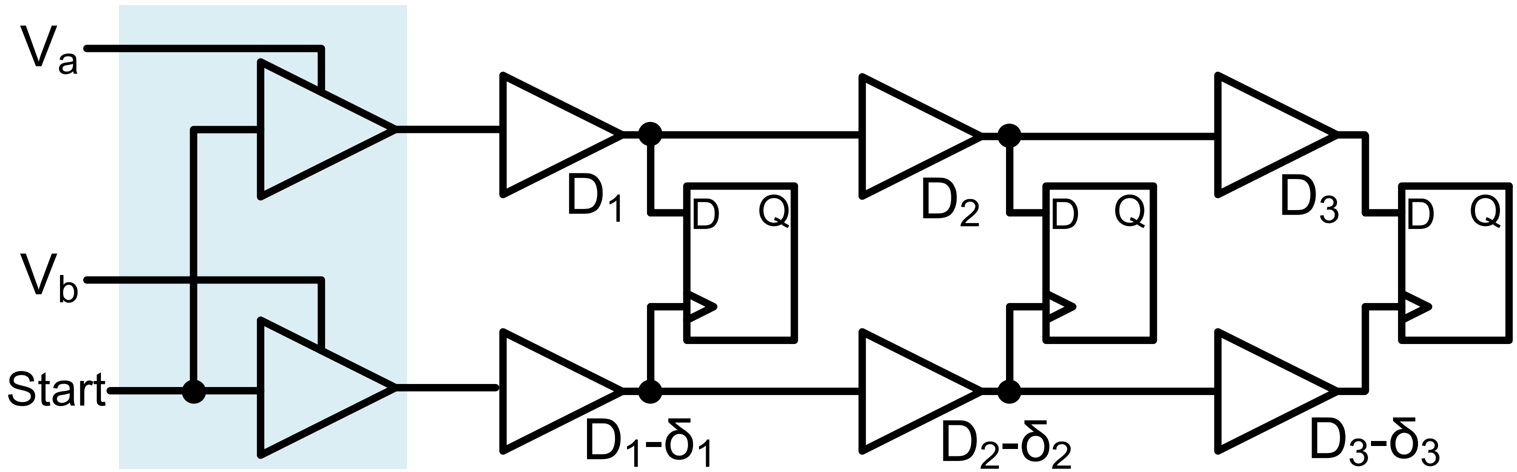
- Variable delay difference, δ_n



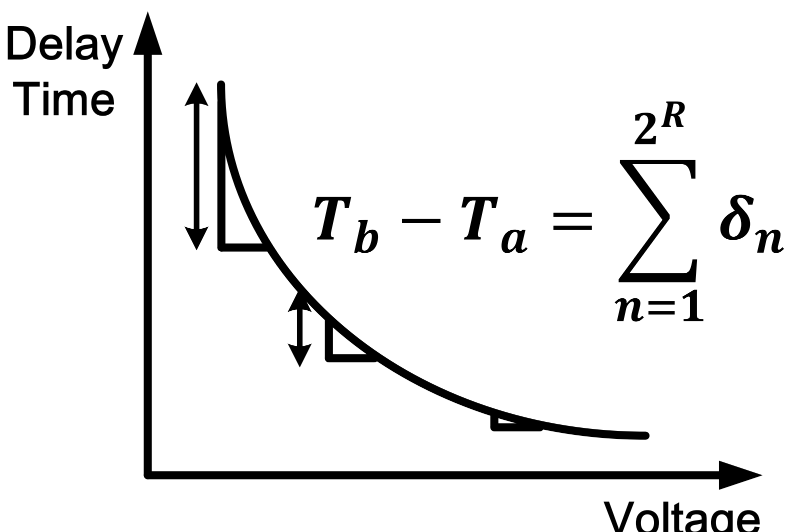
$$T_b - T_a = \sum_{n=1}^{2^R} \delta_n$$



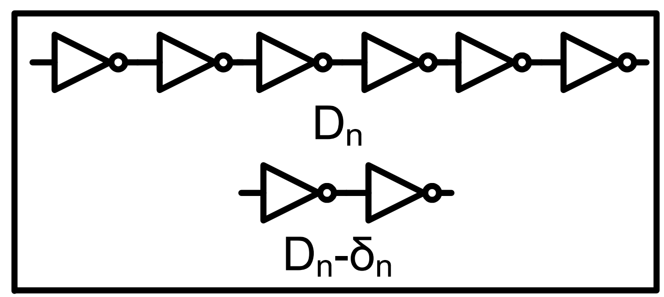
Vernier Time-to-Digital Converter

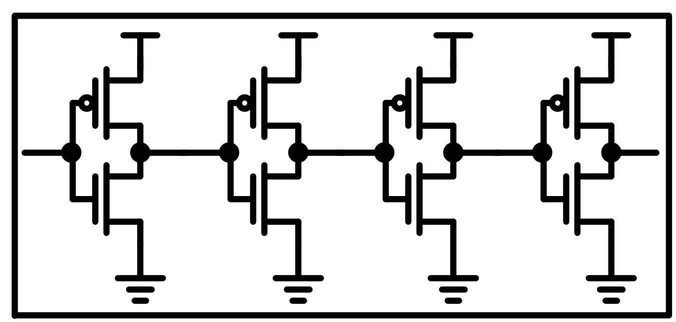


- Variable delay difference, δ_n



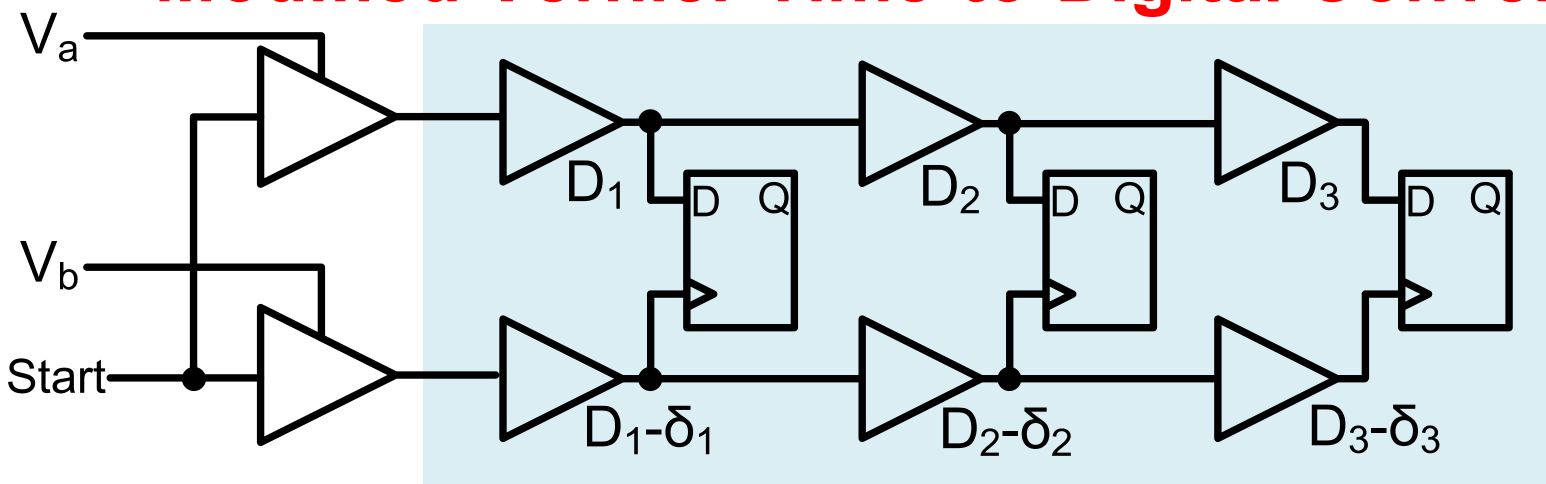
$$T_b - T_a = \sum_{n=1}^{2^R} \delta_n$$



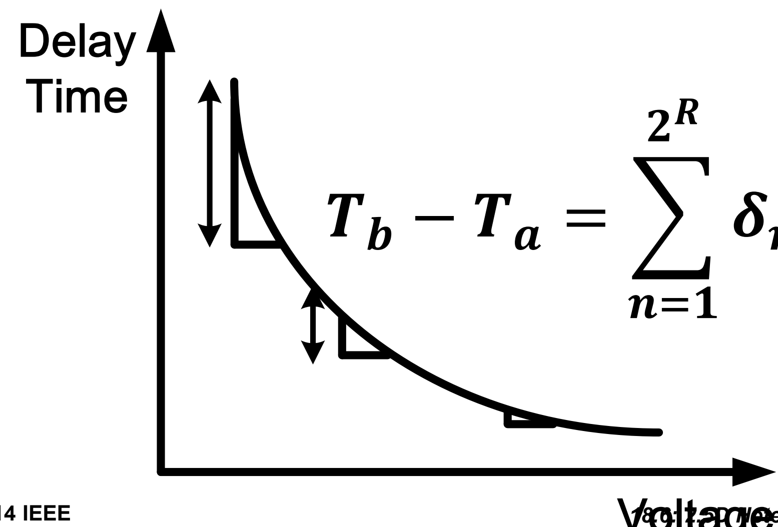


Vernier Time-to-Digital Converter

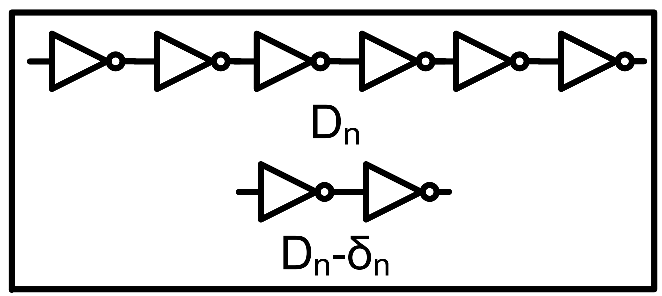
Modified Vernier Time-to-Digital Converter

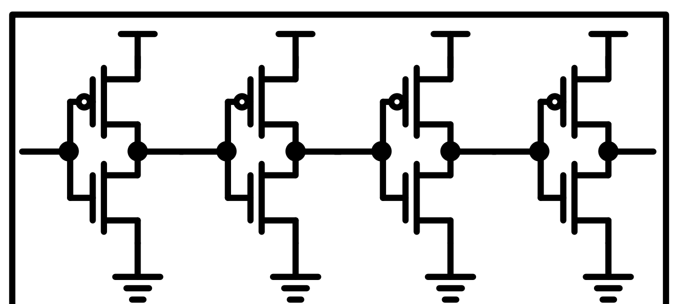


- Variable delay difference, δ_n



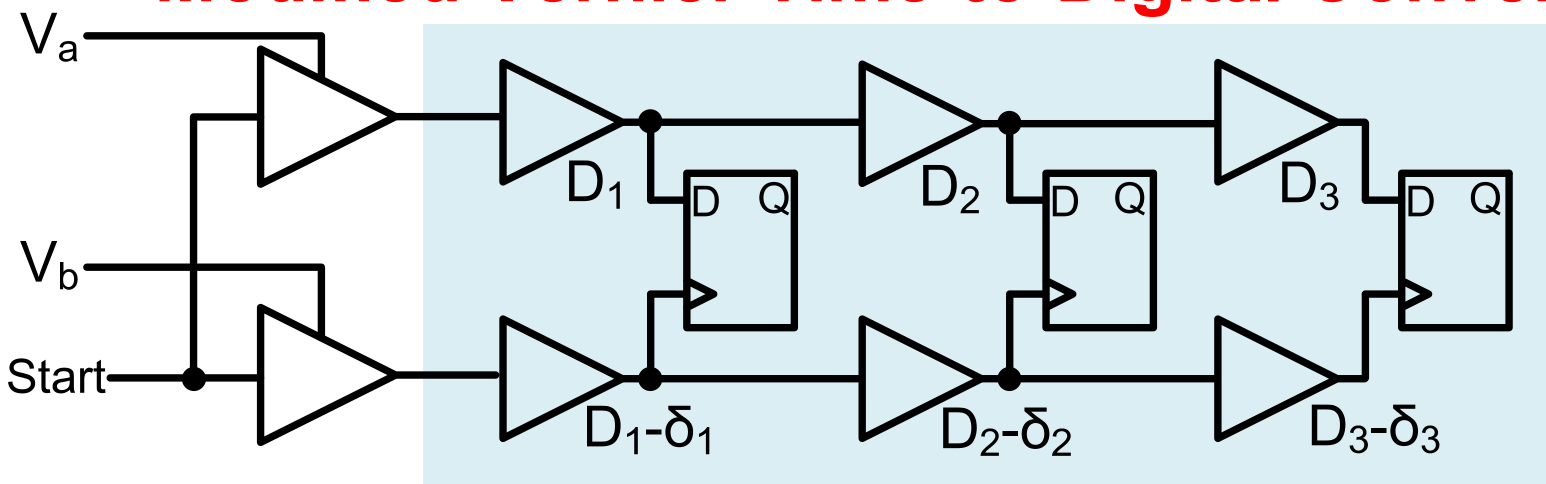
$$T_b - T_a = \sum_{n=1}^{2^R} \delta_n$$



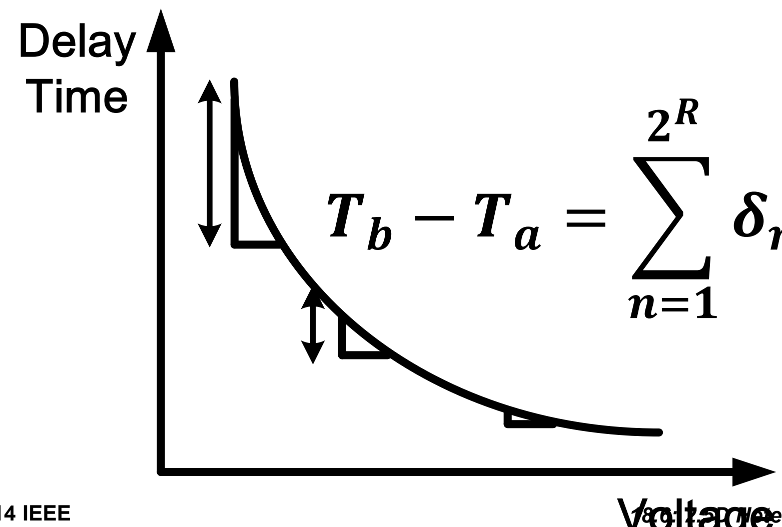


Vernier Time-to-Digital Converter

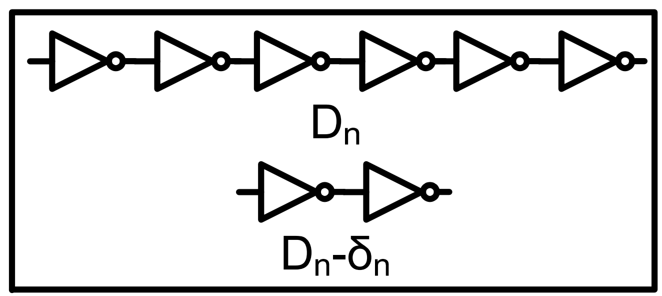
Modified Vernier Time-to-Digital Converter

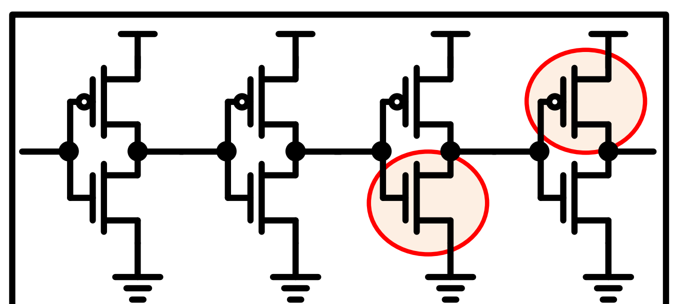


- Variable delay difference, δ_n



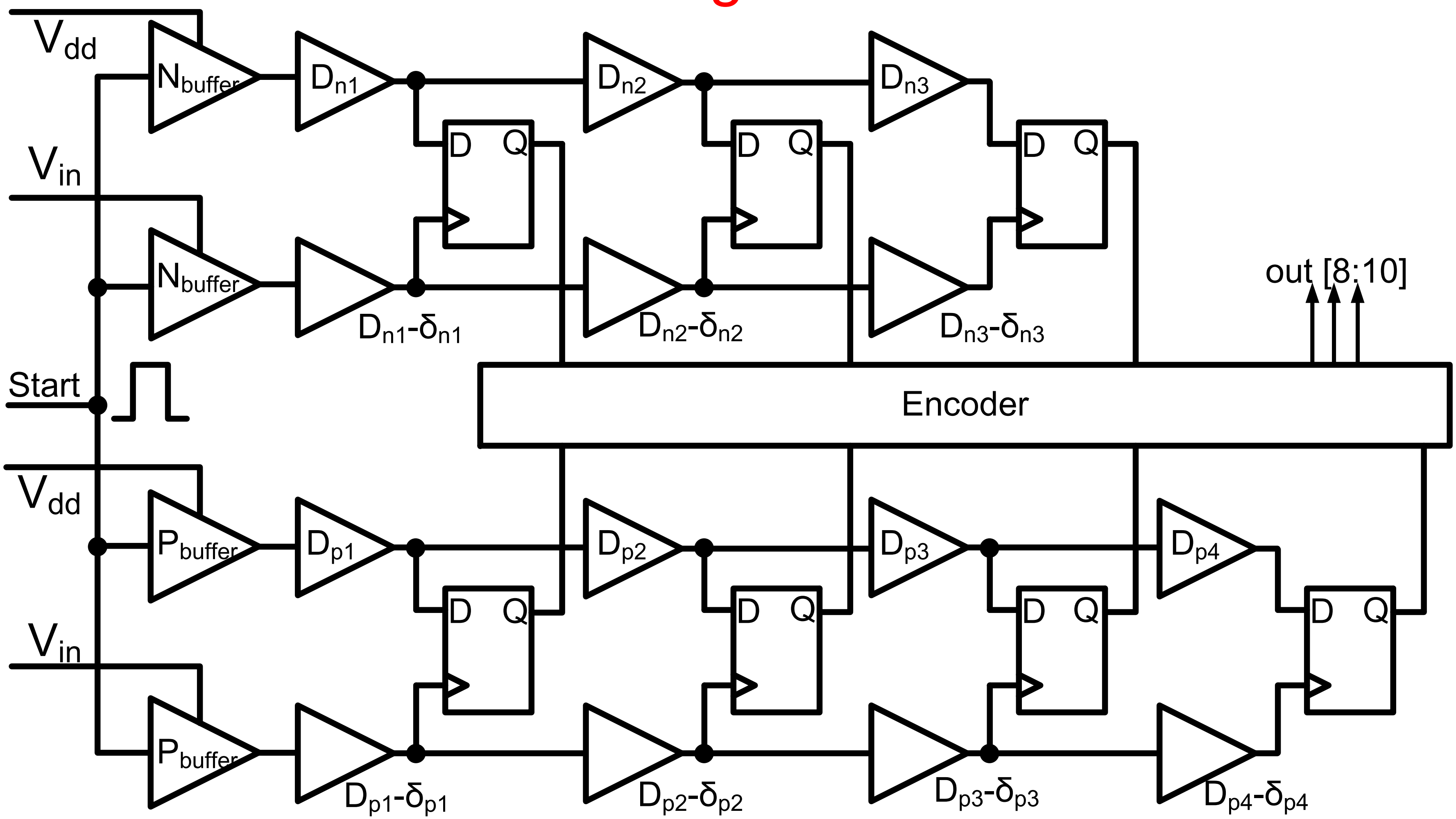
$$T_b - T_a = \sum_{n=1}^{2^R} \delta_n$$





Delay-Line Enhanced Tuning Block

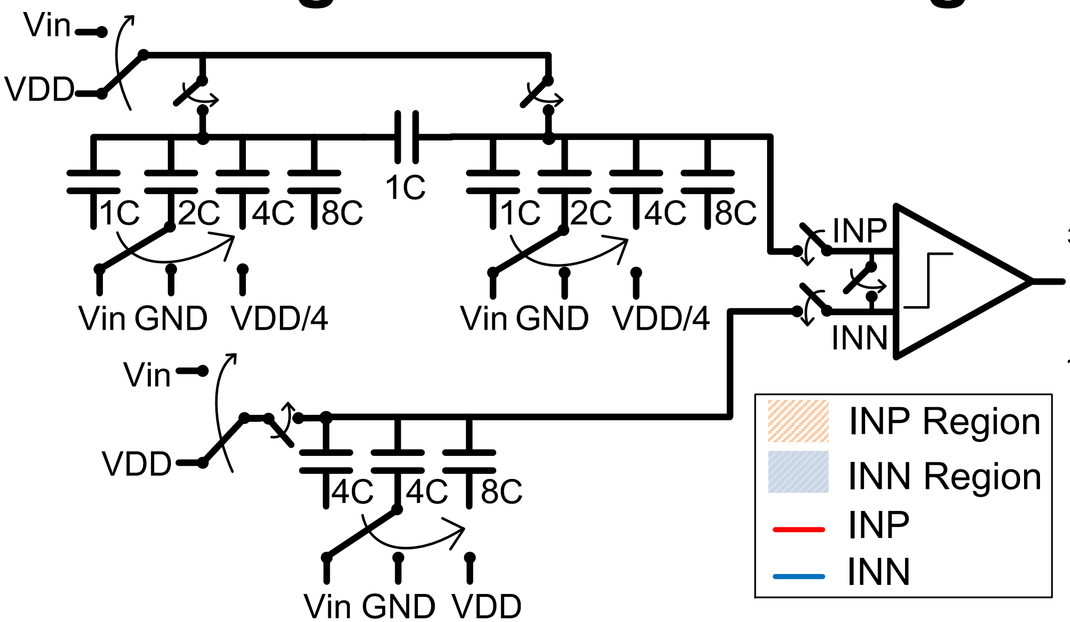
Detection Range: 0.9V ~ 1.8V

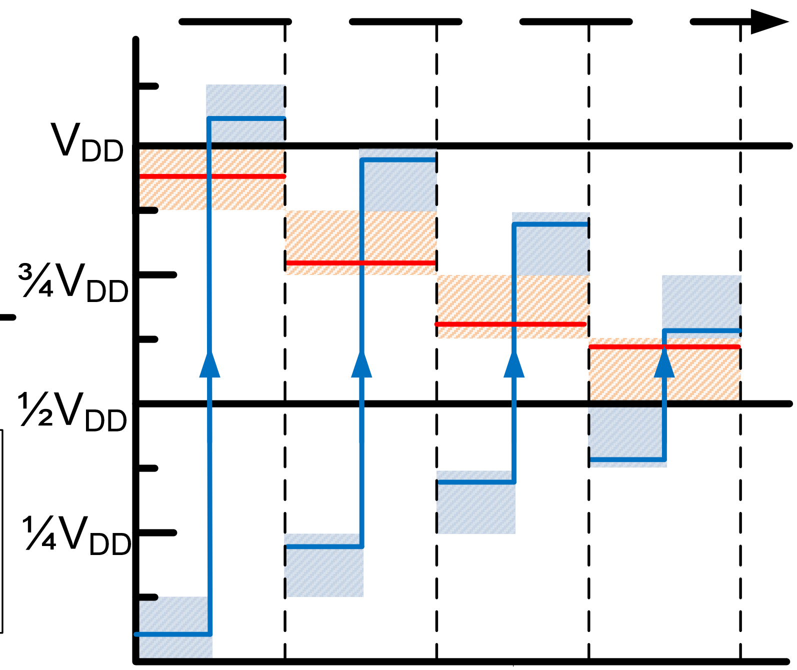


Detection Range: 0V ~ 0.9V

8-Bit SAR ADC for Fine-Tuning

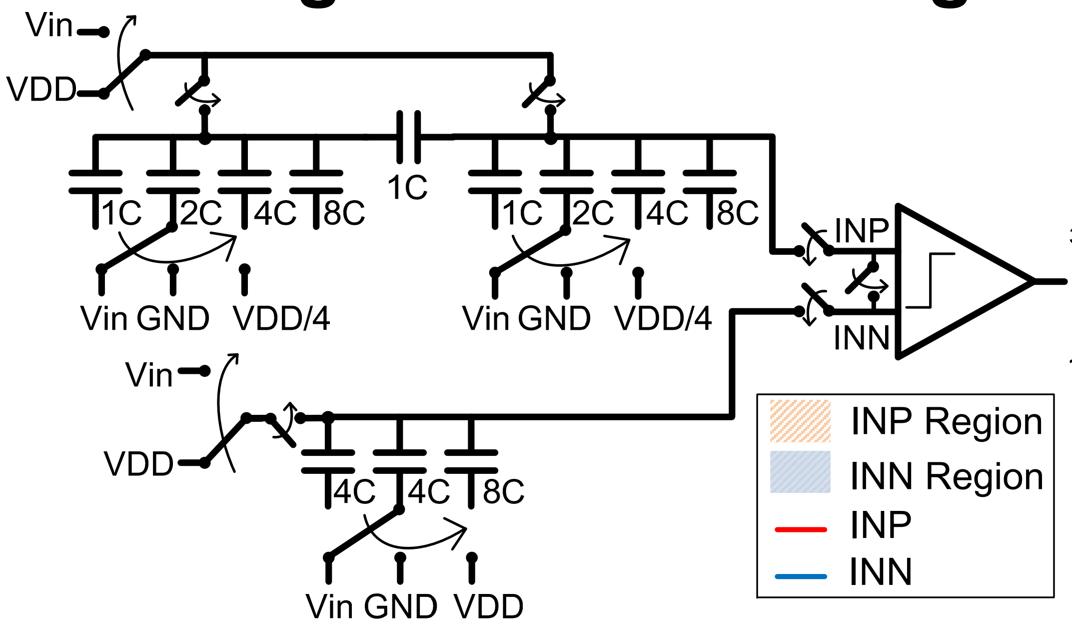
- **Lifting-Based Searching**

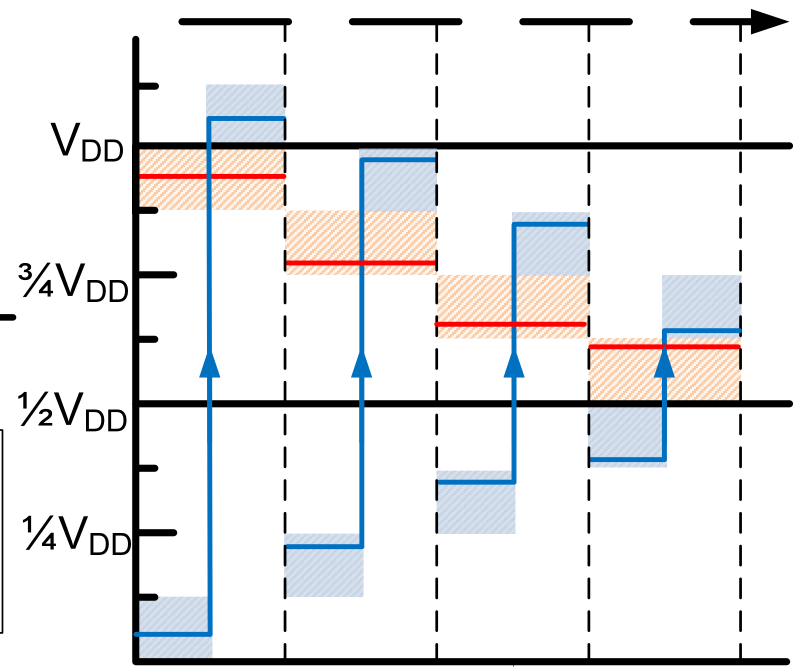




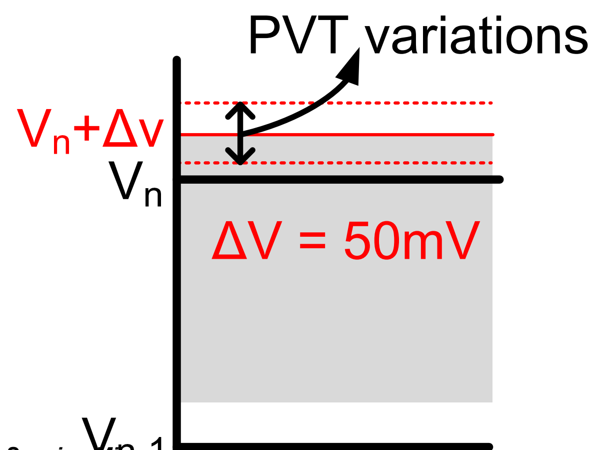
8-Bit SAR ADC for Fine-Tuning

- **Lifting-Based Searching**



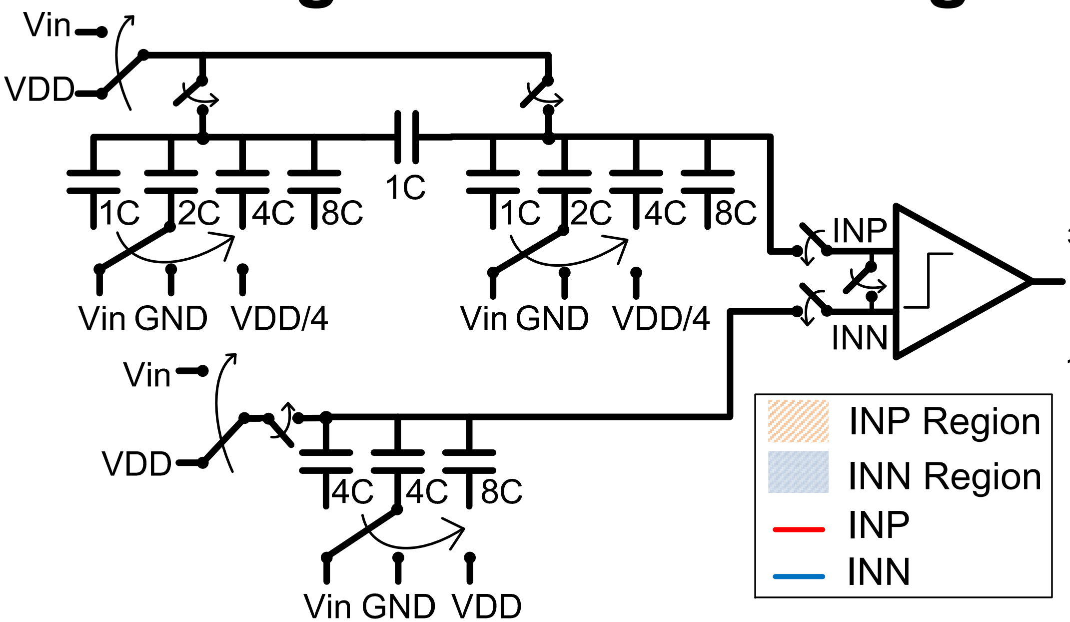


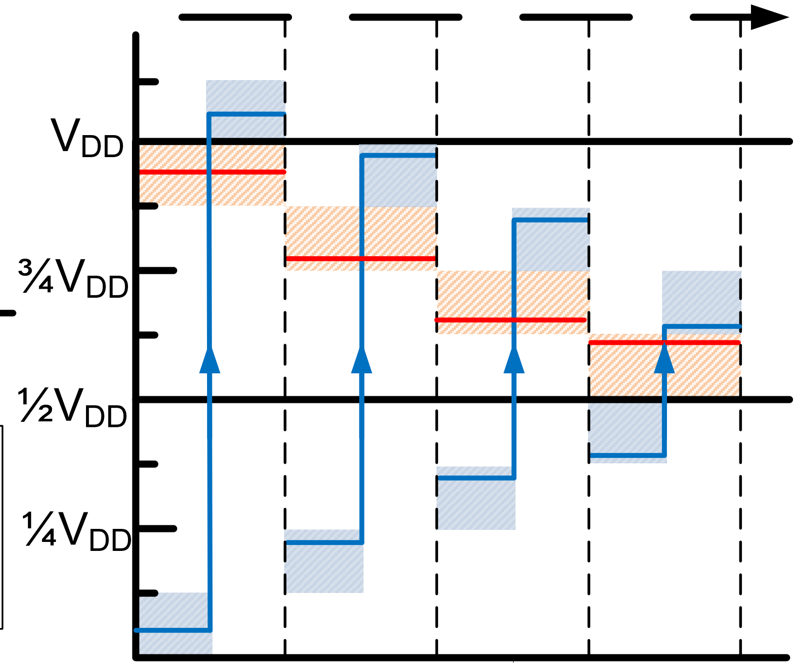
- **Re-Comparison Procedure**



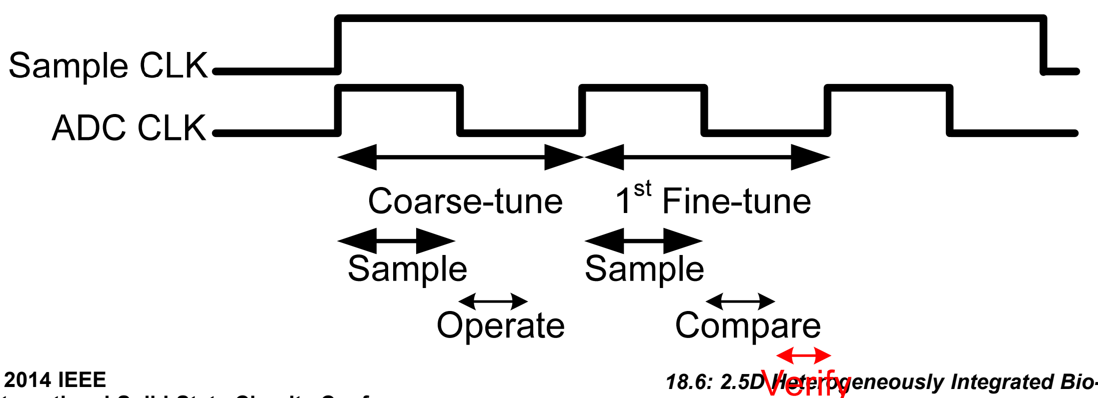
8-Bit SAR ADC for Fine-Tuning

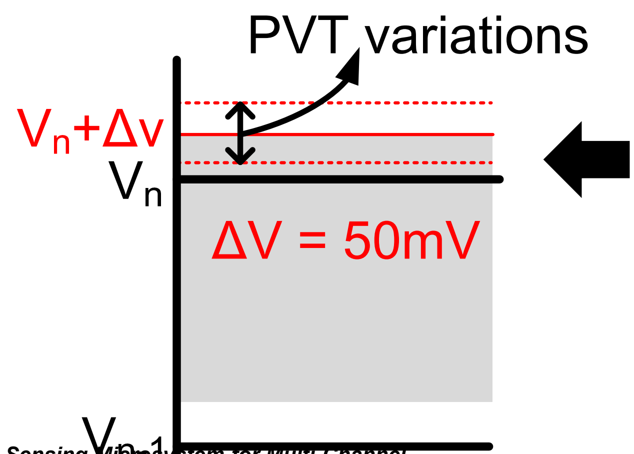
- **Lifting-Based Searching**





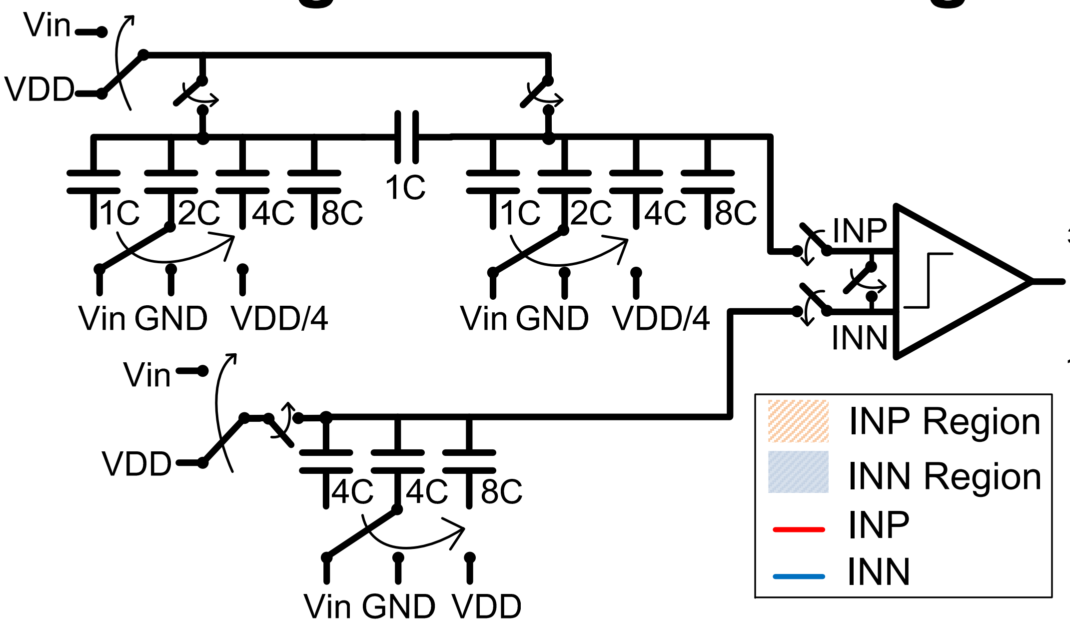
- **Re-Comparison Procedure**

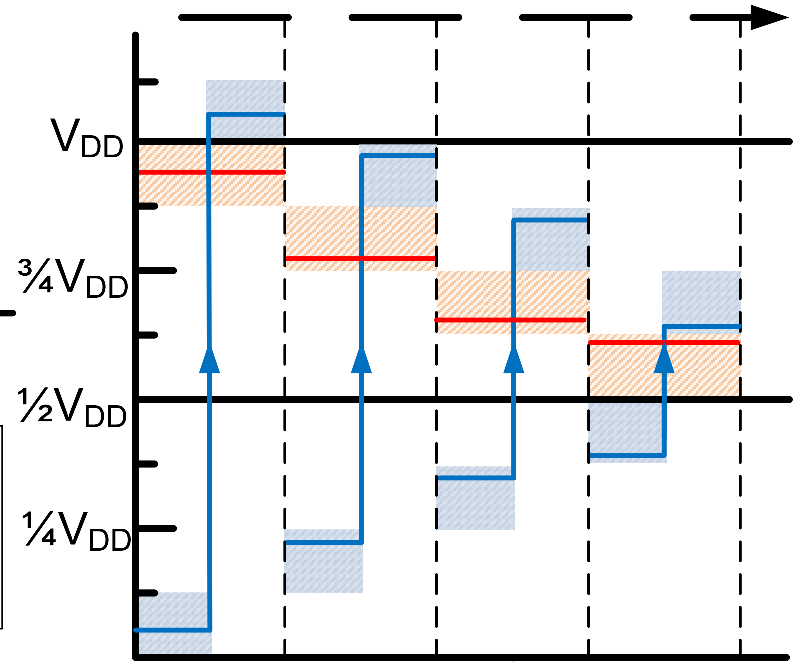




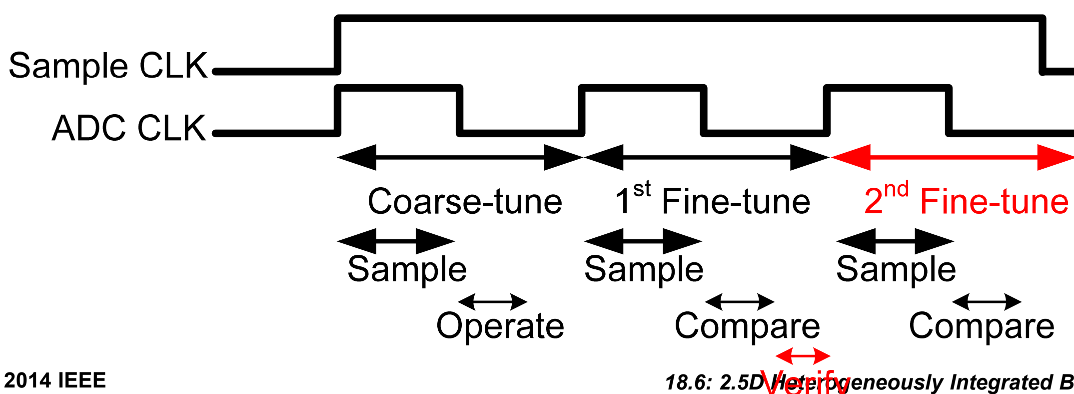
8-Bit SAR ADC for Fine-Tuning

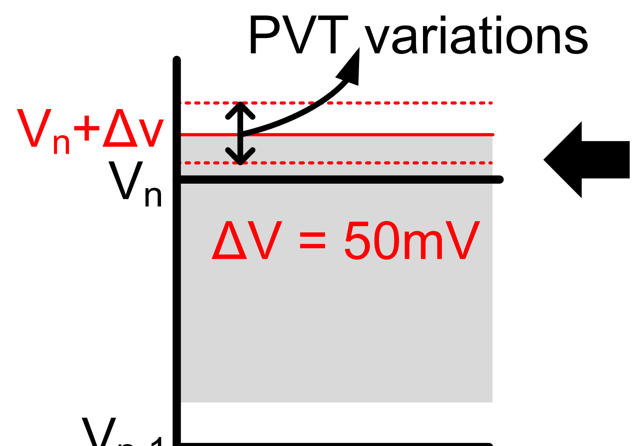
- **Lifting-Based Searching**





- **Re-Comparison Procedure**

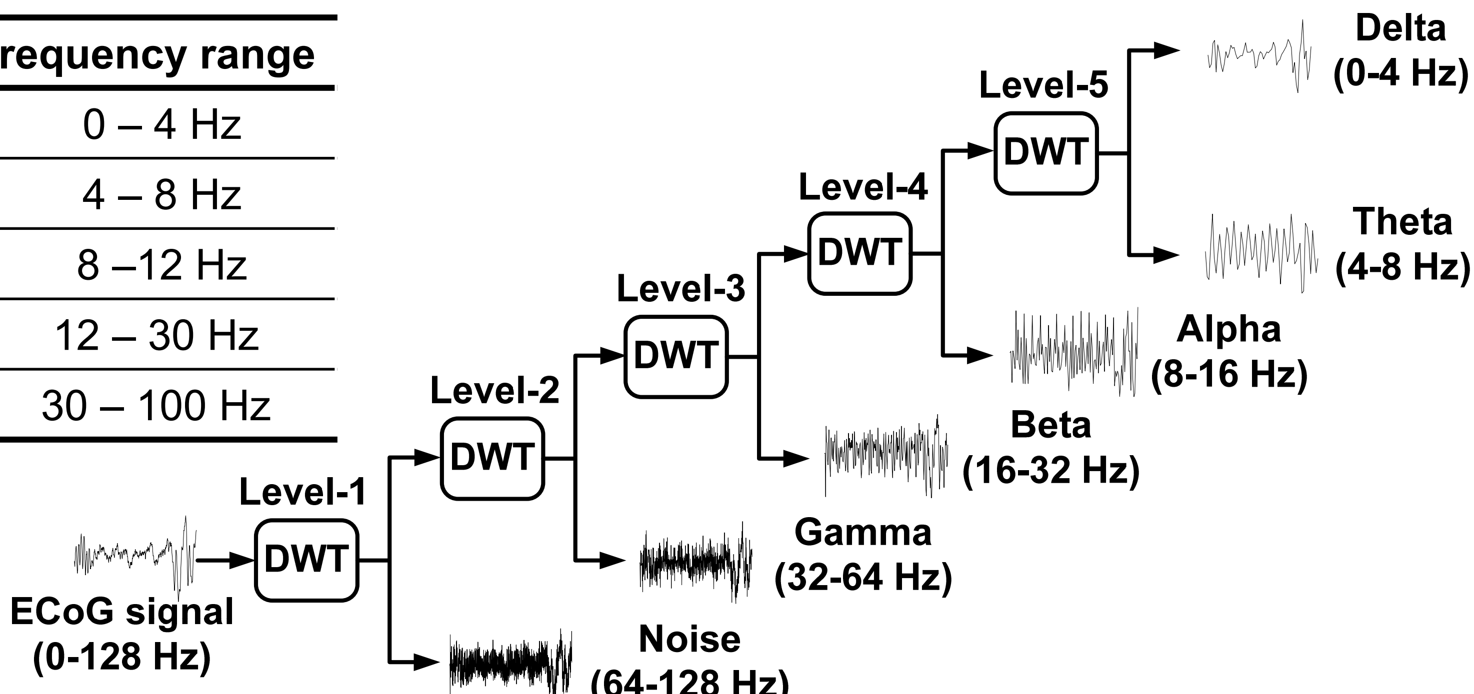




Multi-Level Lifting-Based DWT

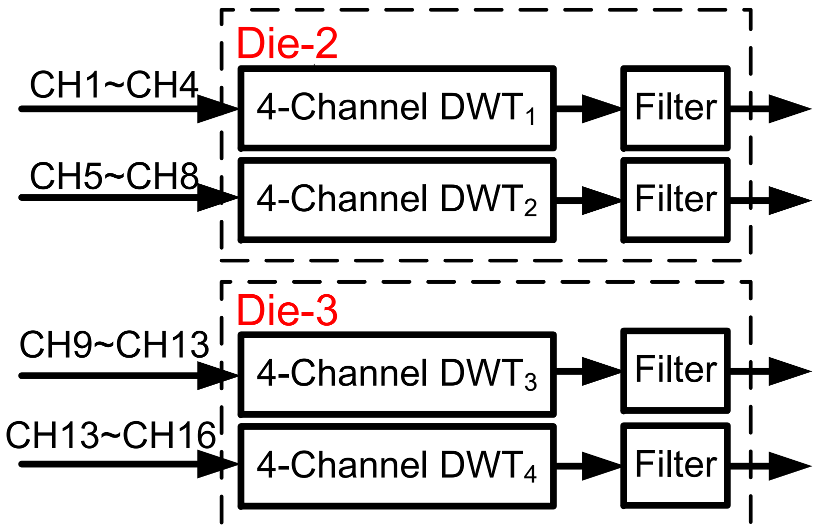
- Multi-level DWT for different frequency bands
- Configurable DWT for different applications
  - Haar, Daubechies-2 (Db2), Symlet-4 (Sym4), Symlet-6 (Sym6)

Wave type	Frequency range
Delta	0 – 4 Hz
Theta	4 – 8 Hz
Alpha	8 –12 Hz
Beta	12 – 30 Hz
Gamma	30 – 100 Hz



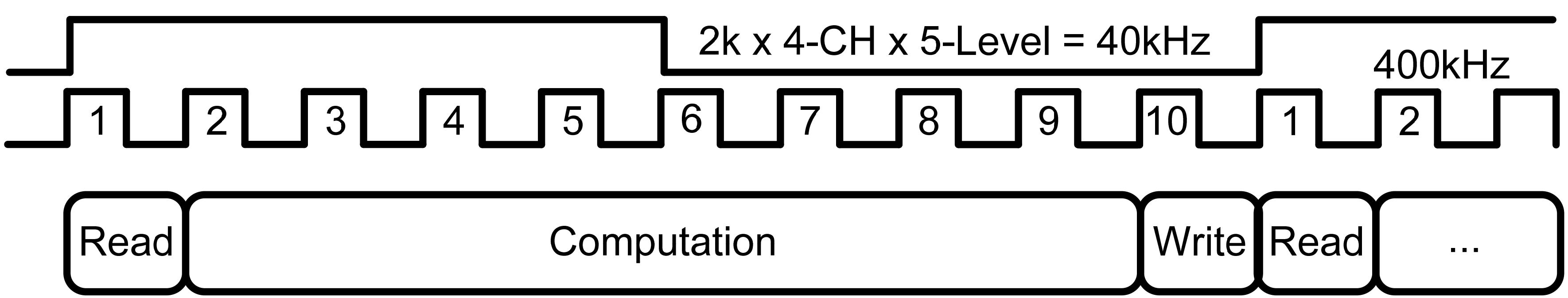
Implementation of 16-CH DWT

- 4 folded time-multiplexing 4-CH DWTs for 16-CH (Area-power optimization)



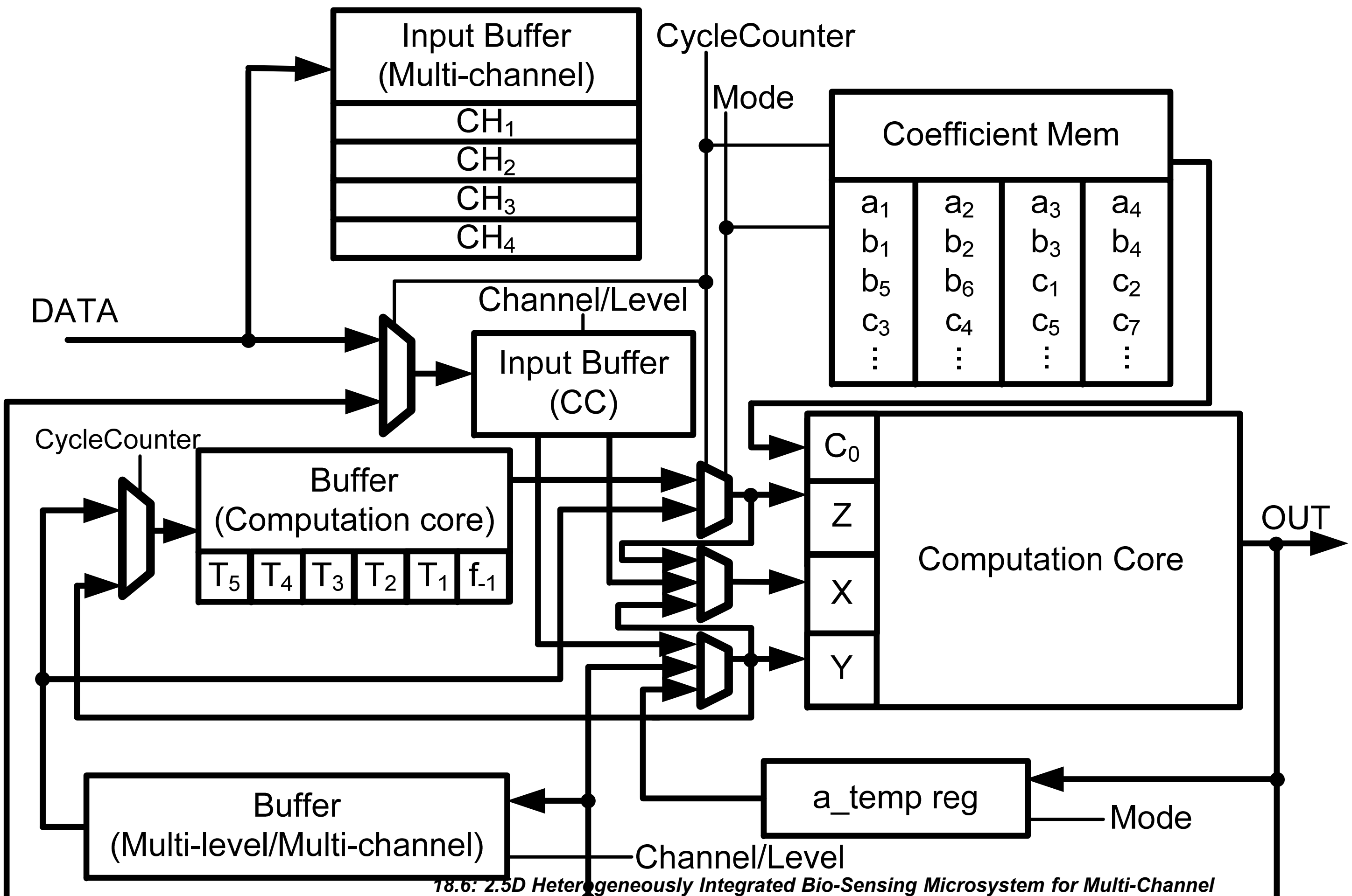
Sampling rate of 1-CH: 2kHz
Input data rate for 4-CH: 8kHz

<u>Timing Diagram of 1-Level Iteration (8 computation cycles)</u>



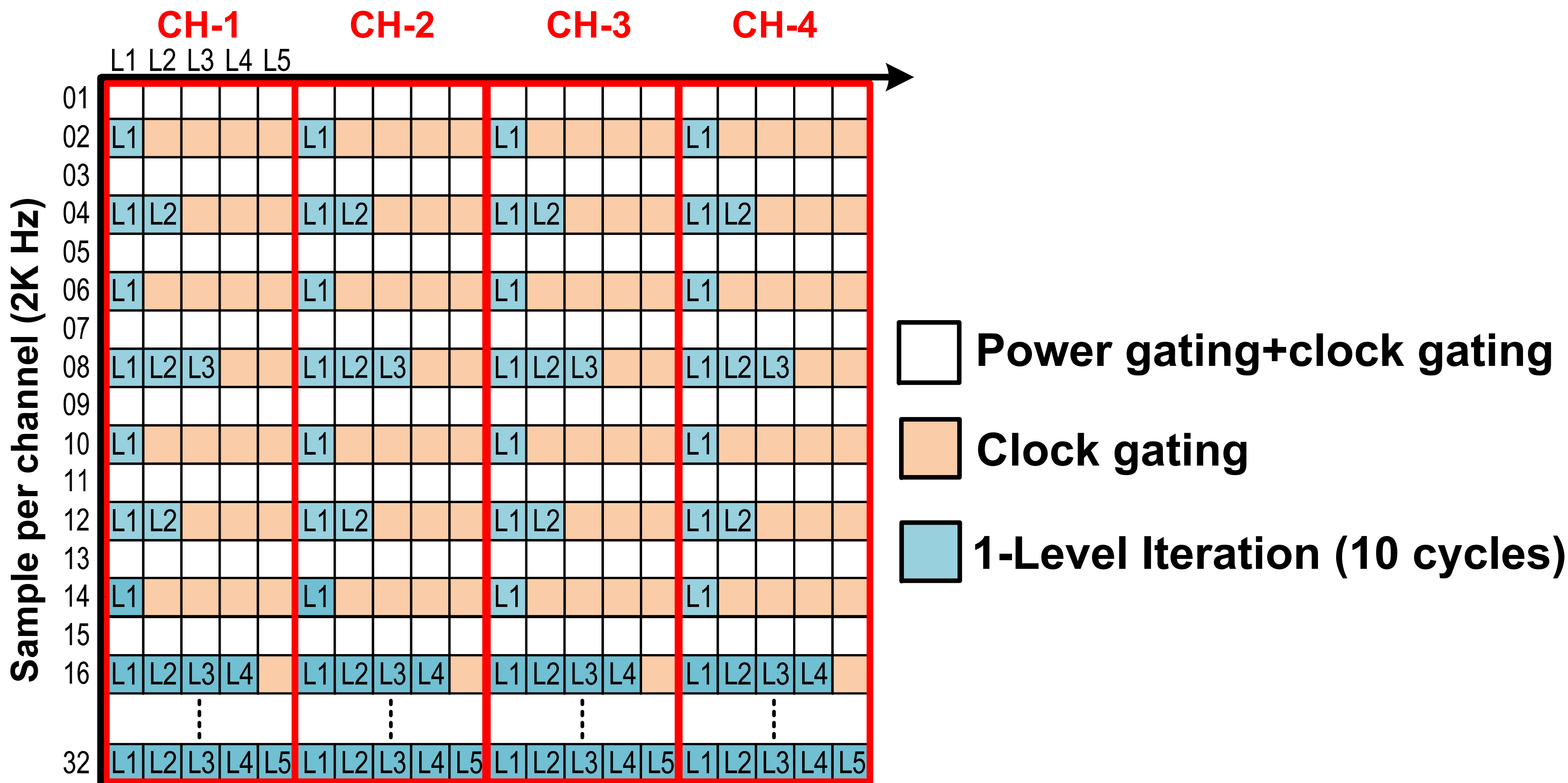
Architecture of 4-CH DWT

- Configurable 4-CH DWT
  - Different frequency-bands & mother wavelets



Clock/Power Gating for 4-CH DWT

- Power gating for leakage power reduction
- Clock gating for dynamic power saving

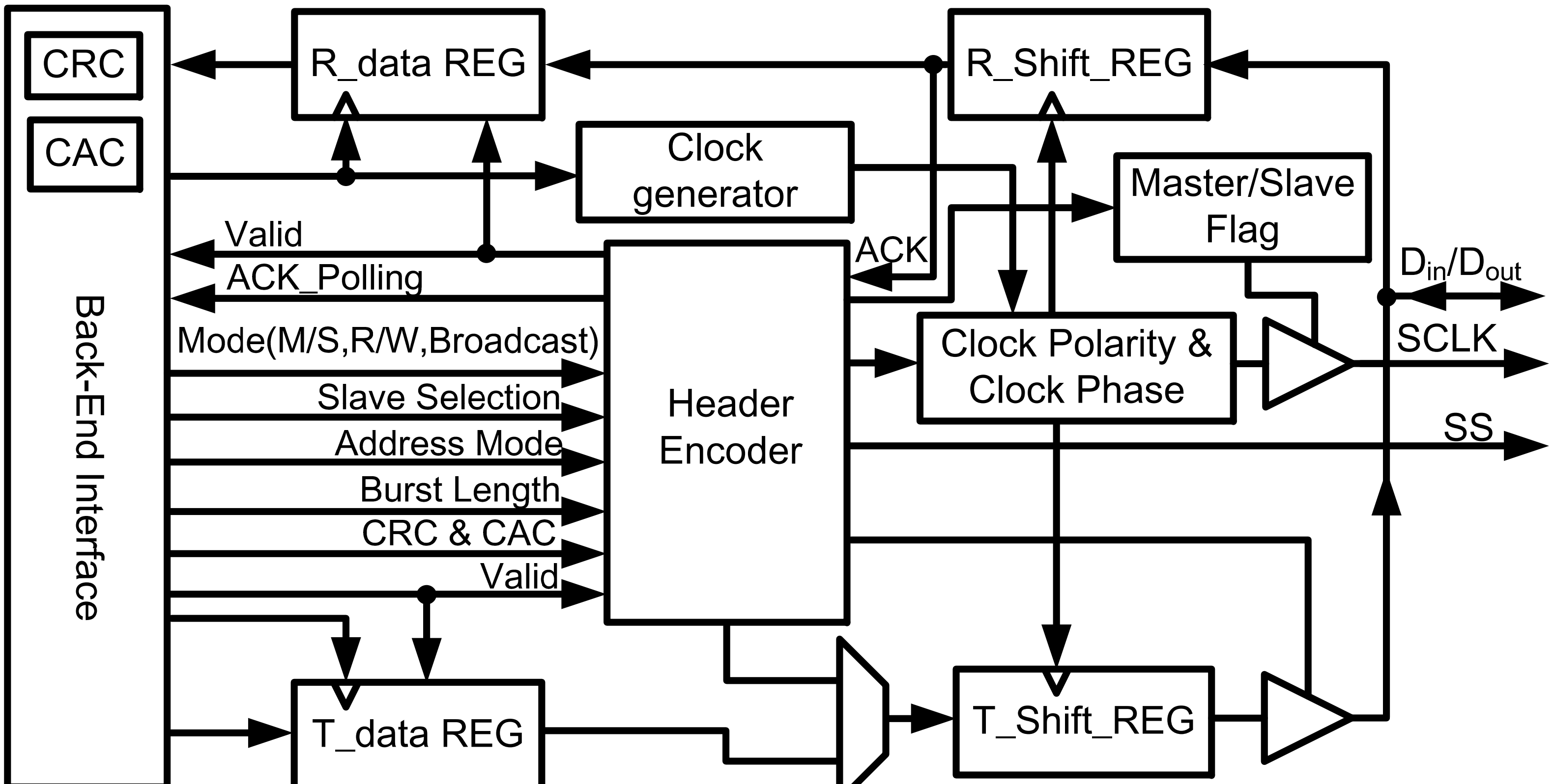


On-Interposer Bus, μ-SPI

- **Parallel interface**
  - 1-bit data -> 1-to-4 data width with 1 clock pin
- **Pseudo multi-master**
- **Hierarchical header for packetization of μ-SPI**
  - Half/Full duplex
  - Point-to-Point/Broadcasting
  - Variable-width of burst length
  - Receive-controlled ACK
- **Error correction & low power bus coding options**
  - CRC: Cyclic redundancy check
  - CAC: Crosstalk avoidance code

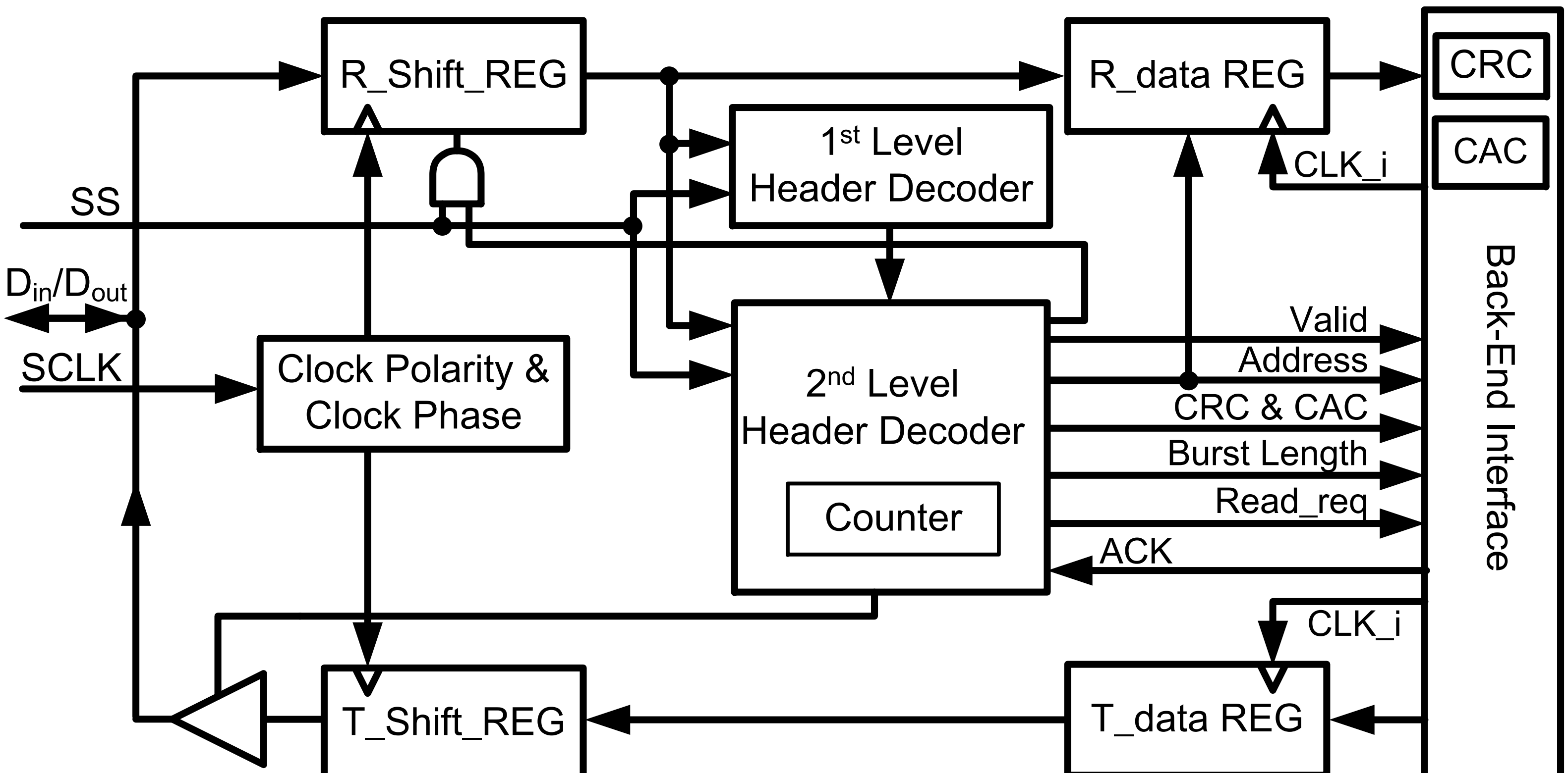
Master of μ-SPI

- Header encoder
- Bus clock generator
- MS_flag = 1



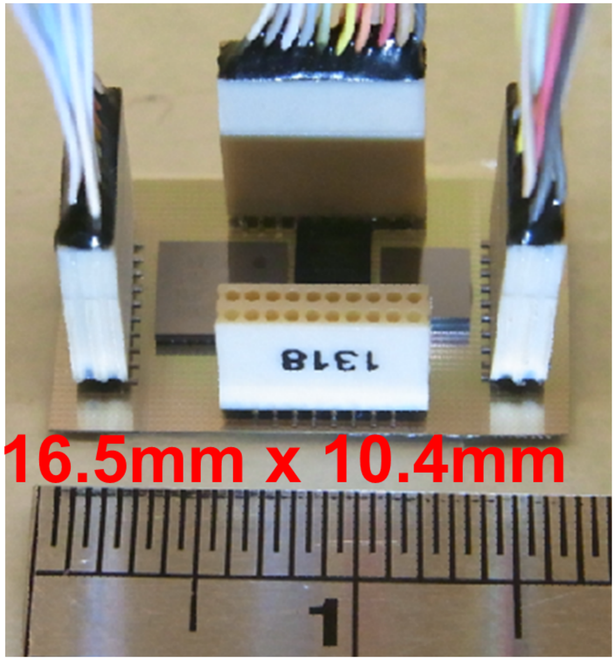
Slave of μ-SPI

- 2-Level decoder
- Receive-Controlled ACK

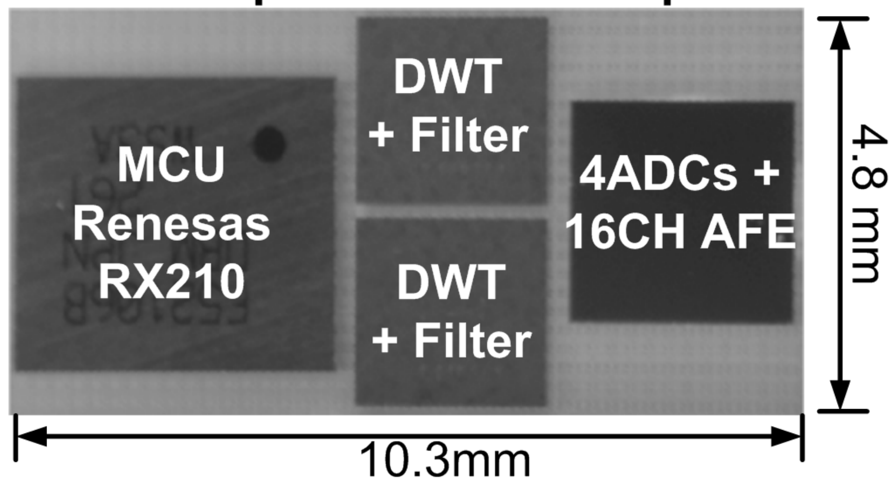


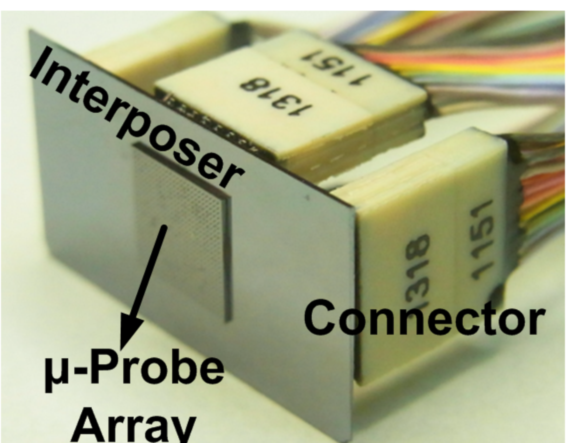
Micrographs of 2.5D Microsystem

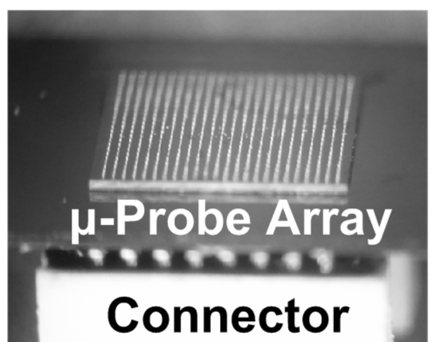
Bio-Sensing Microsystem

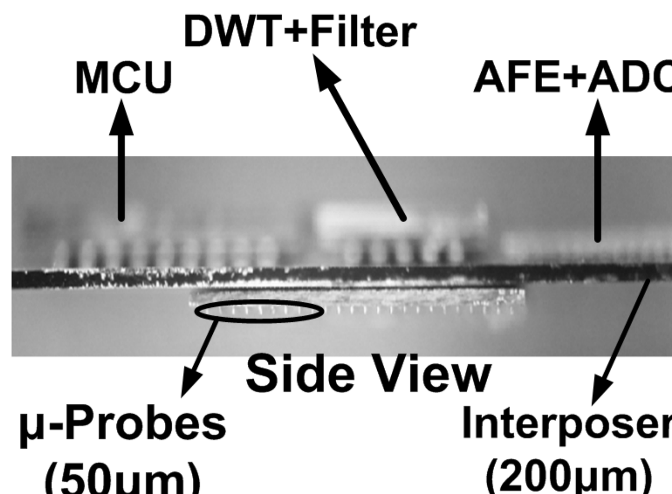


Die Floorplan on 2.5D Interposer

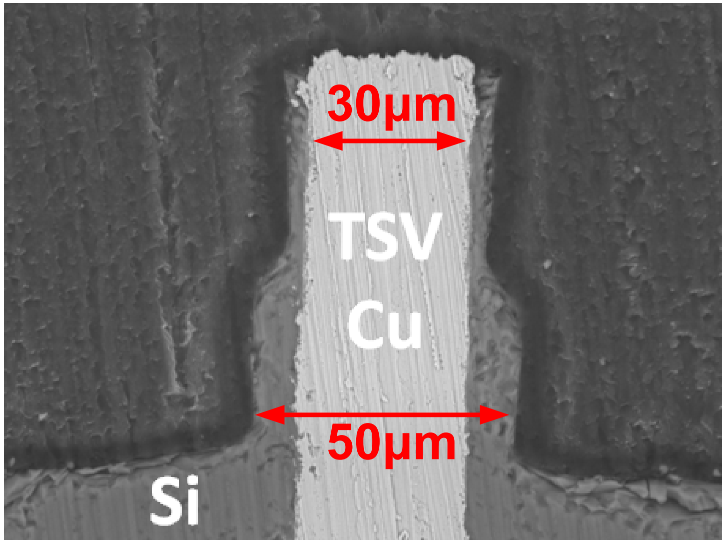


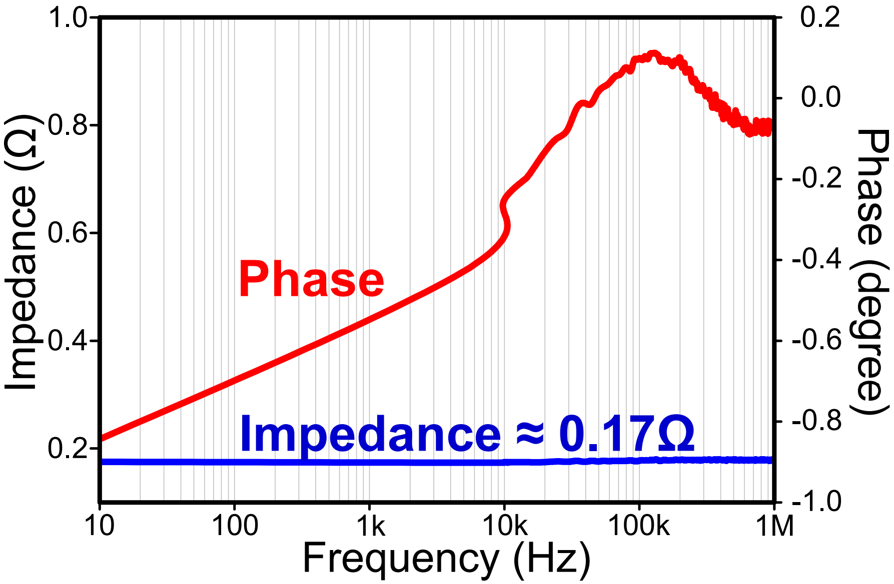


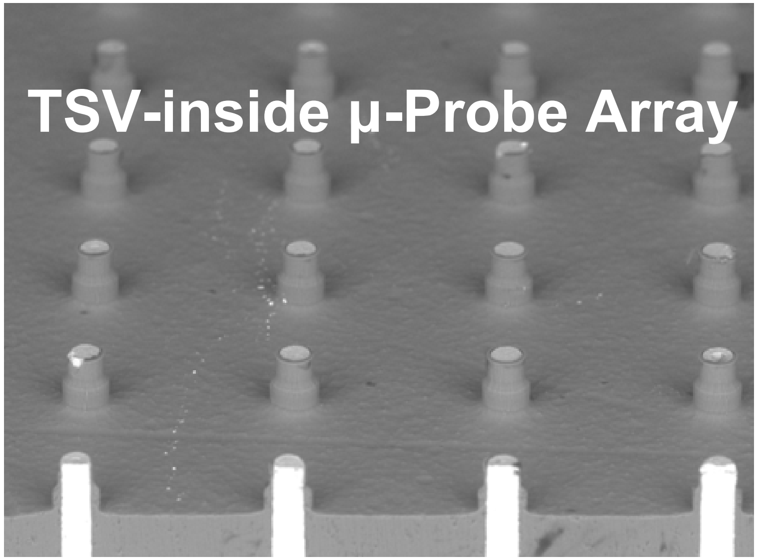


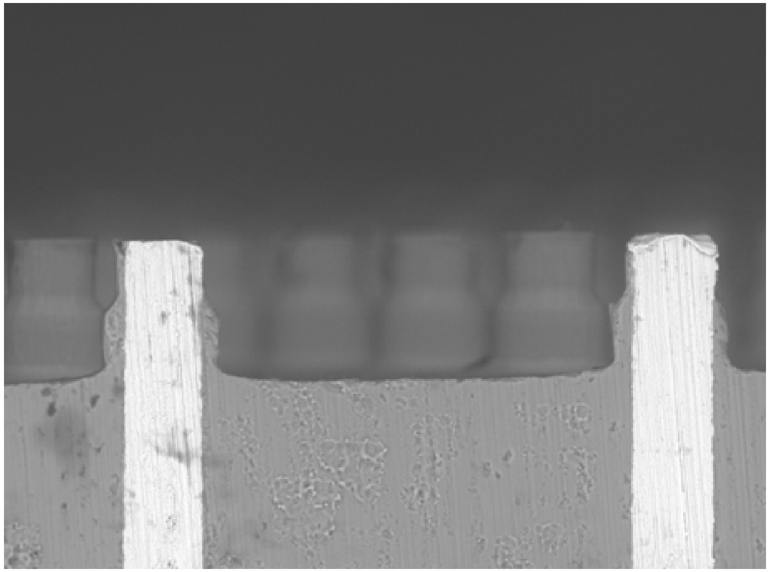


TSV-inside μ-Probes

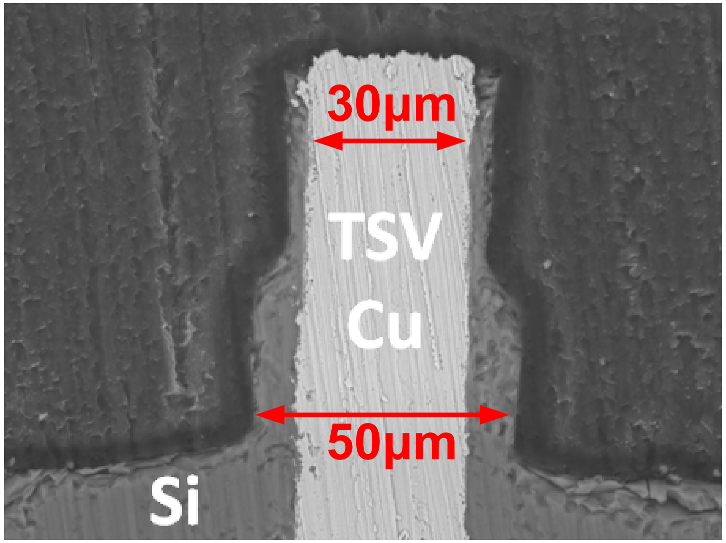


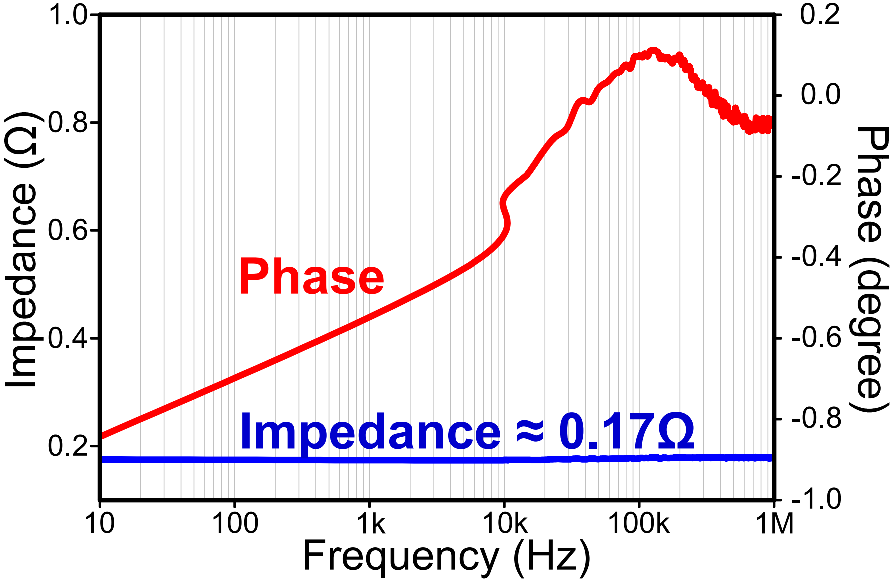


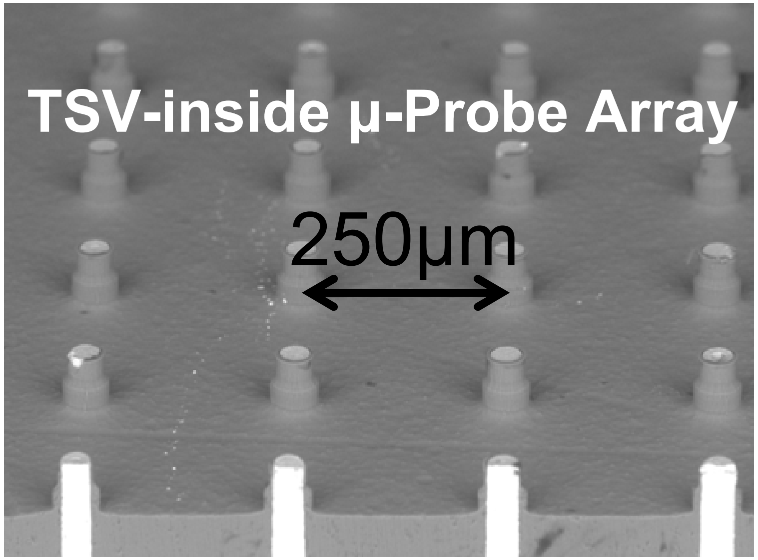


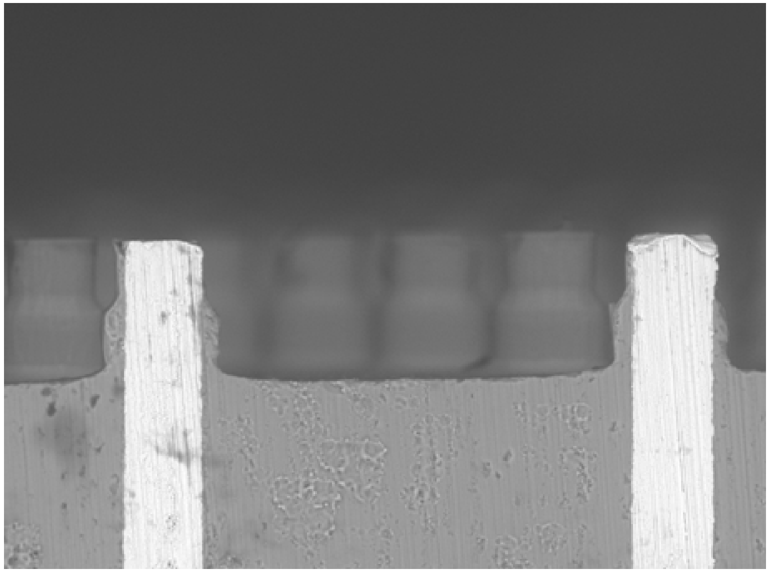


TSV-inside μ-Probes

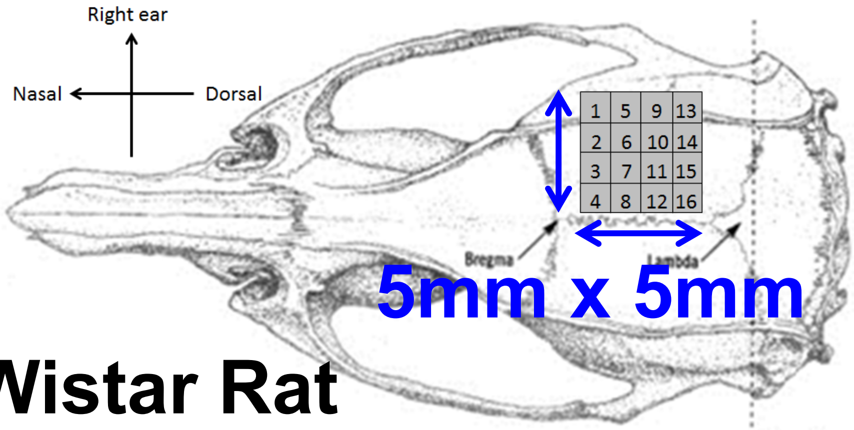




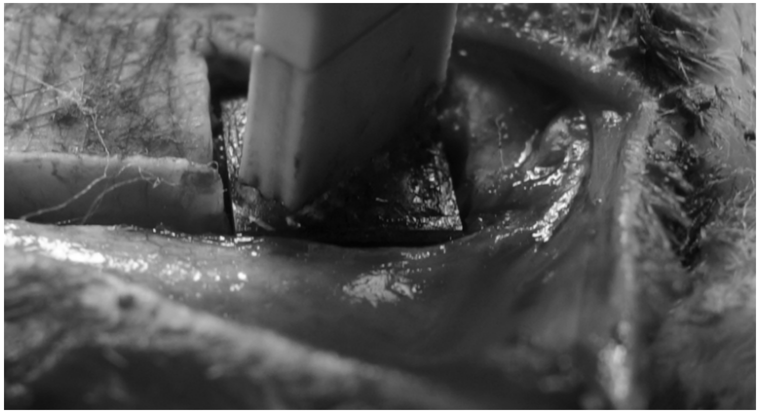


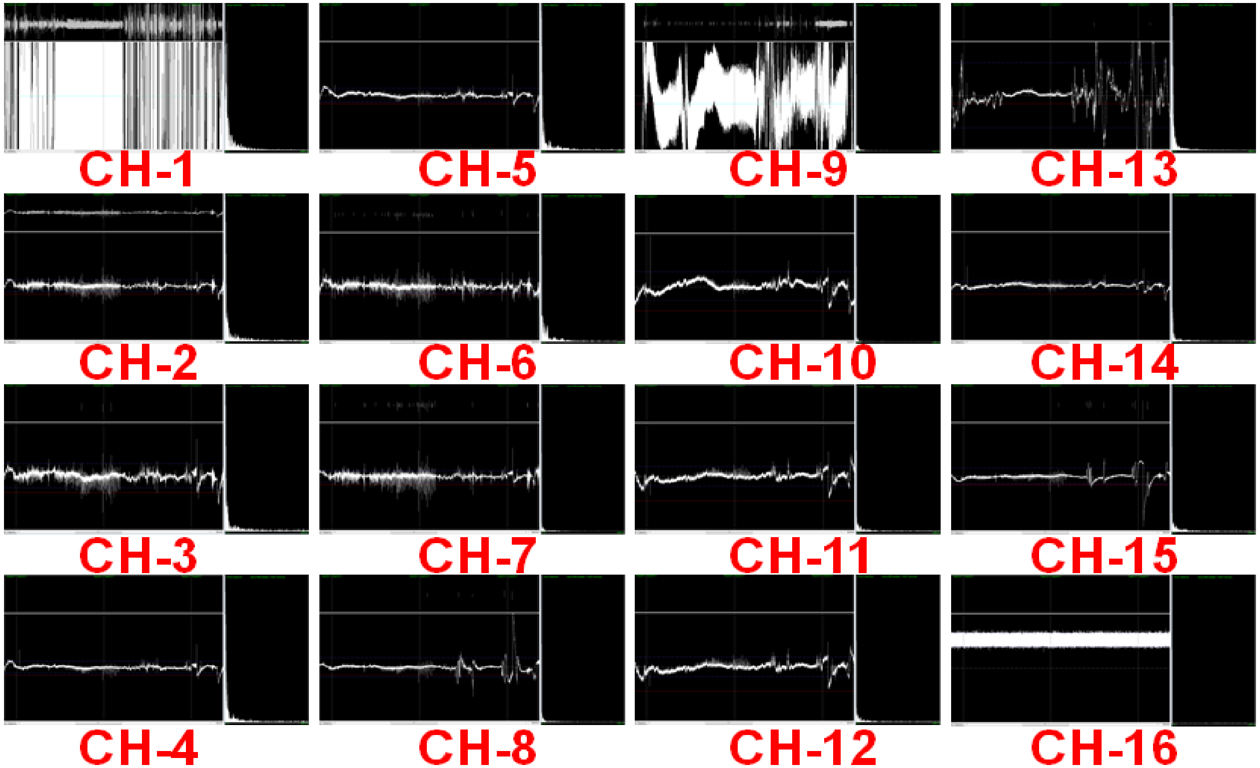


µ-Probe Mechanical Strength Test

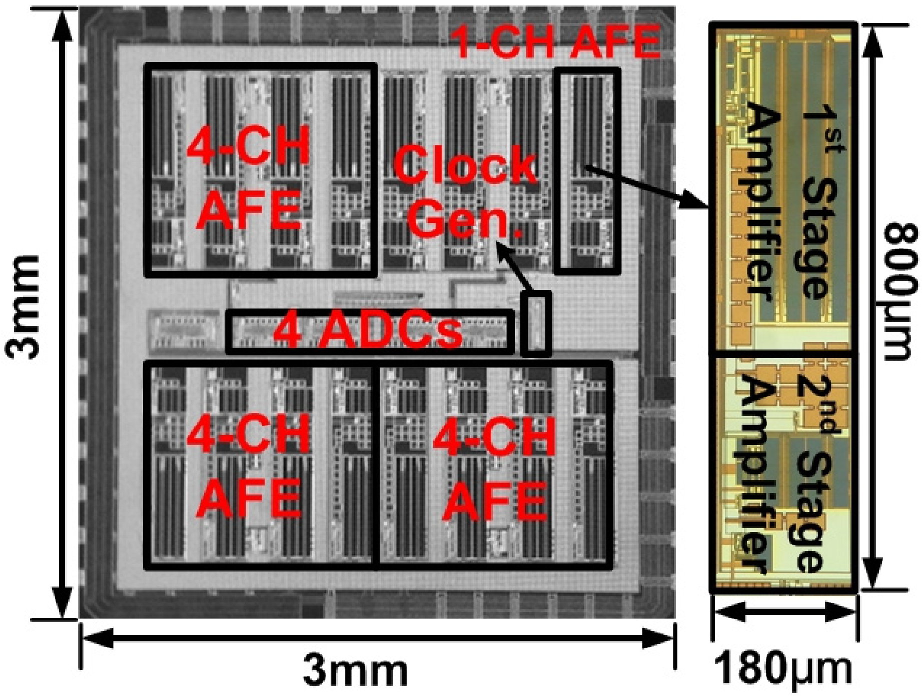


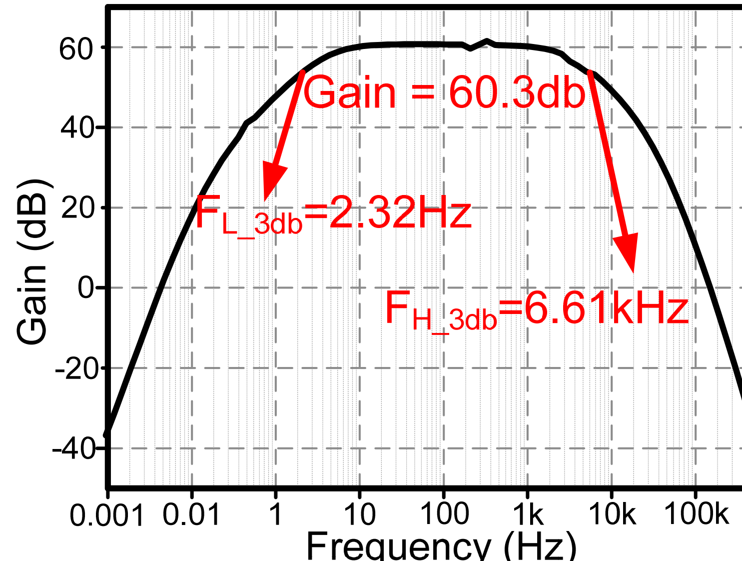
Wistar Rat

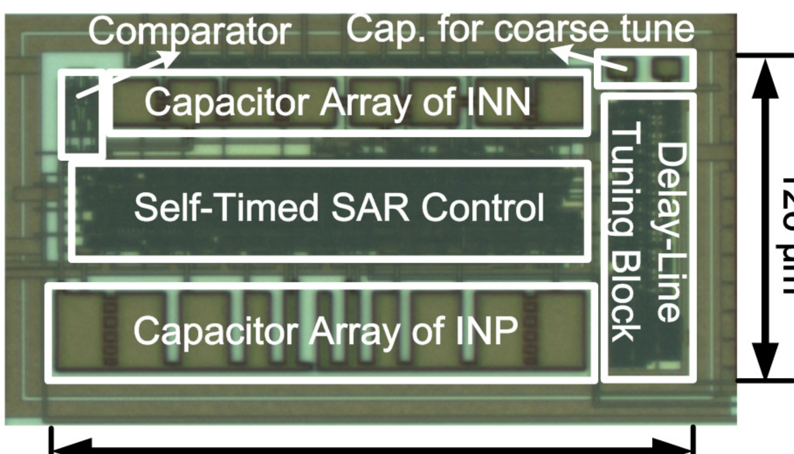


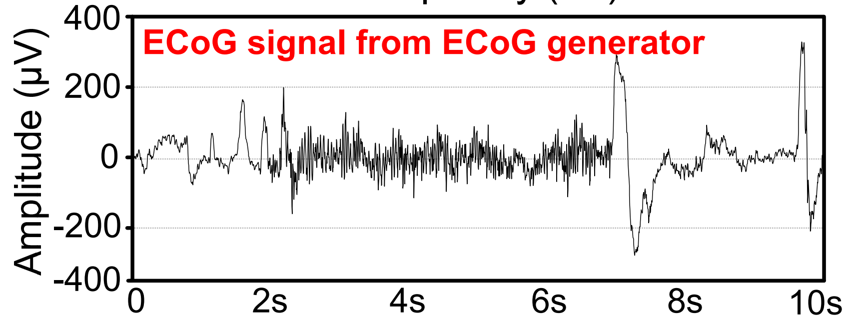


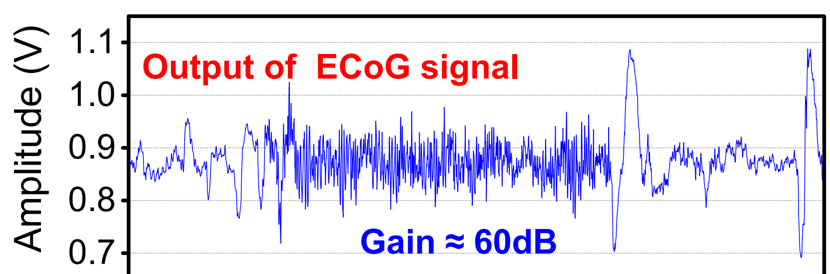
16-Channel μ-ECoG Acquisition





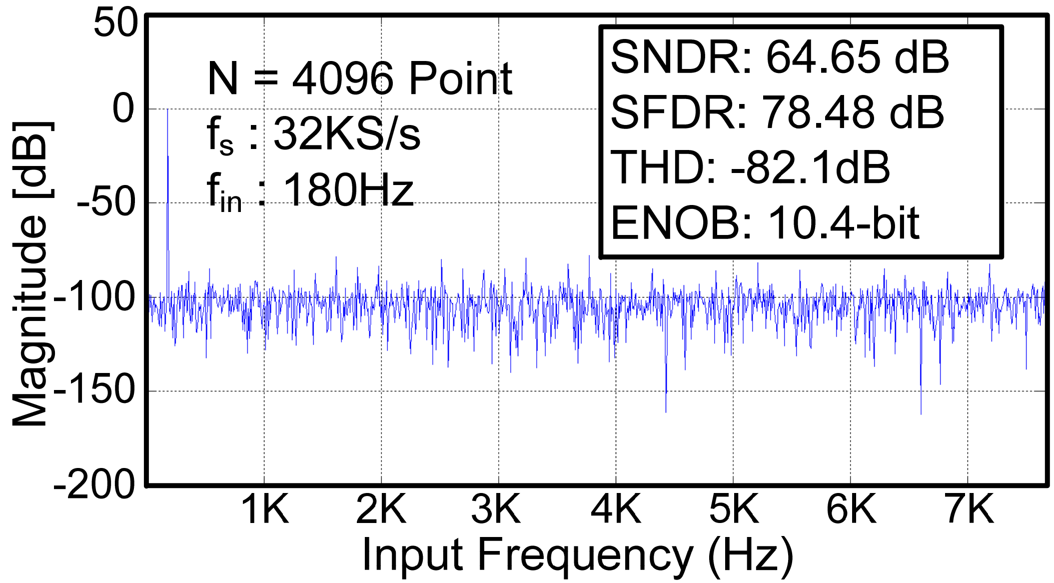


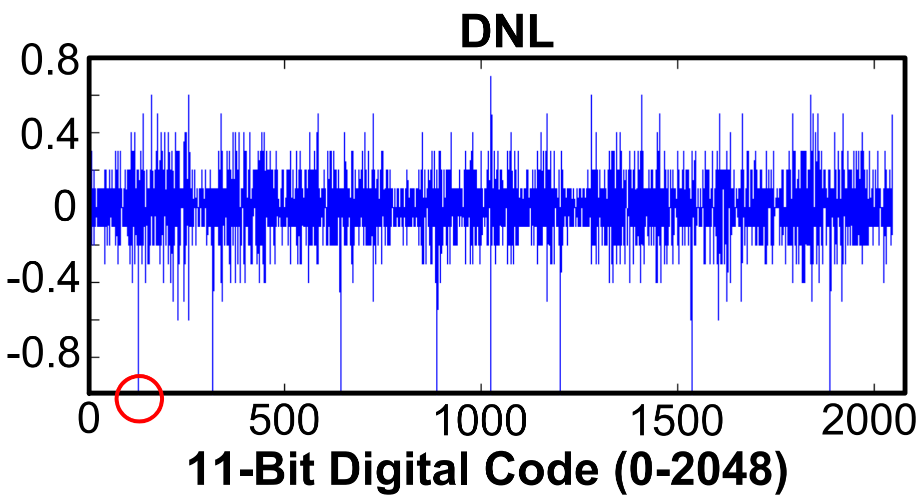




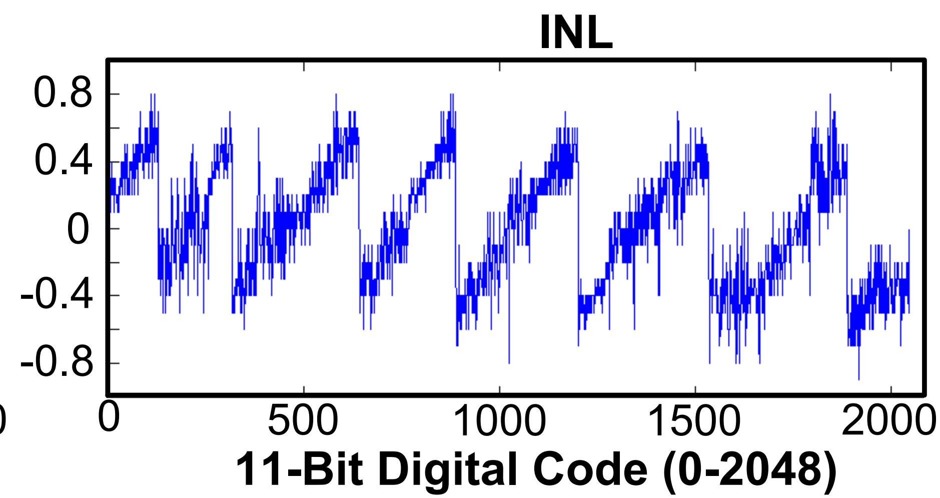
Characteristics of 11-Bit ADC

- 42% area reduction compared with ordinary SAR ADC





+0.7/-1.0 LSB



+0.8/-0.9 LSB

Comparison of Microsystems

ISSCC'13	This Work
TSV-Based Double-Side Integrated Microsystem	**TSV-Based 2.5D Heterogeneously Integrated Microsystem**
<u>Neural Signal Collection</u> 5x6 probes per-channel 3x14 TSVs per-channel	**<u>Neural Signal Collection</u>** Configurable probes per-channel TSV-inside μ-probe
<u>Neural Signal Acquisition</u> 16-Channel AFE	**<u>Neural Signal Acquisition</u>** 1. 16-Channel AFE 2. 11b area-power efficient ADC
N.A.	**<u>Neural Signal Processing</u>** 1. DWT + Filter (Feature Extraction) 2. MCU - Renesas RX210 (Control + Feature Classification)
N.A.	On-interposer bus μ-SPI

Conclusions

- **2.5D heterogeneously integrated bio-sensing microsystem with TSV-inside μ-probes** for μECoG sensing applications
- **Microsystem = μ-probes + 1 interposer + 4 dies**
  - Biopotential acquisition: AFE + area-power-efficient ADCs
  - Feature extraction: Configurable DWTs with power/clock gating in 2 dies
  - System control + feature classification: MCU
- **Low power on-interposer bus (μ-SPI)**
  - Pseudo multi-master, hierarchical header
- **The overall power ⇨ 676.3μW**

ISSCC 2014

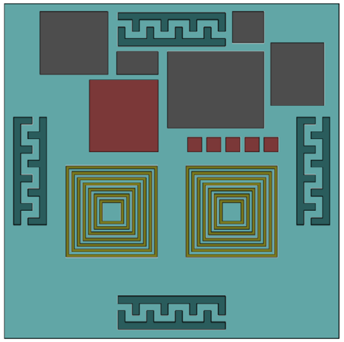
A Remotely-Controlled Locomotive IC Driven by Electrolytic Bubbles and Wireless Powering

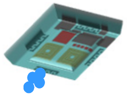
Po-Hung Kuo[1], Jian-Yu Hsieh[1], Yi-Chun Huang[1], Yu-Jie Huang[1], Rong-Da Tsai[2], Tao Wang[3], Hung-Wei Chiu[2], Shey-Shi Lu[1]

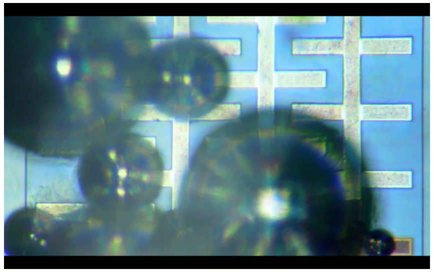
[1]National Taiwan University
[2]National Taipei University of Technology
[3]Chang Gung University

Outline

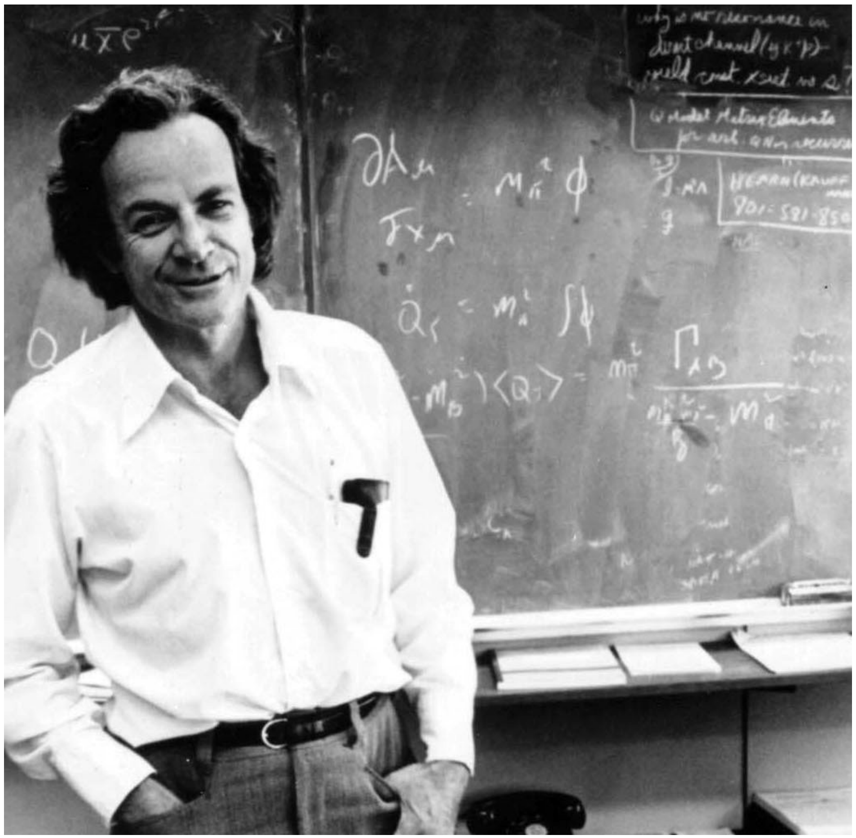
- Introduction
- Issues of System Design
- Circuit Design
- Experimental Results
- Conclusions







Richard Feynman



There's Plenty of Room at the Bottom

(Dec. 29, 1959)

“the weird possibility of swallowing the doctor”

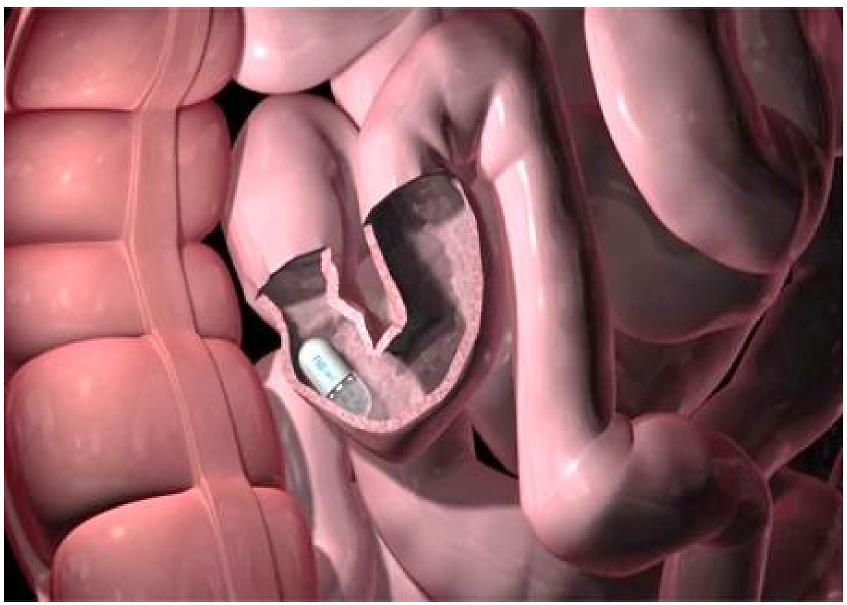
Reference:
http://jonathanbaldwin.co.uk/doctor-who/

Beyond the "Fantastic Voyage (1966)"

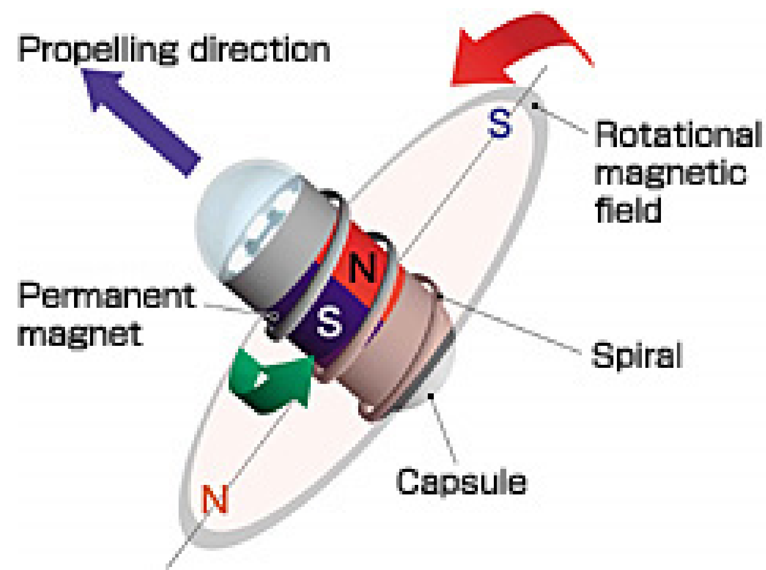
Reference:
http://convergence.ucsb.edu/files/issues/convergence-14/voyage.jpg

Propulsive Force

- Magnetic Actuation (Capsule Endoscopy)
- Lorenz Force
- Electrolytic Bubble



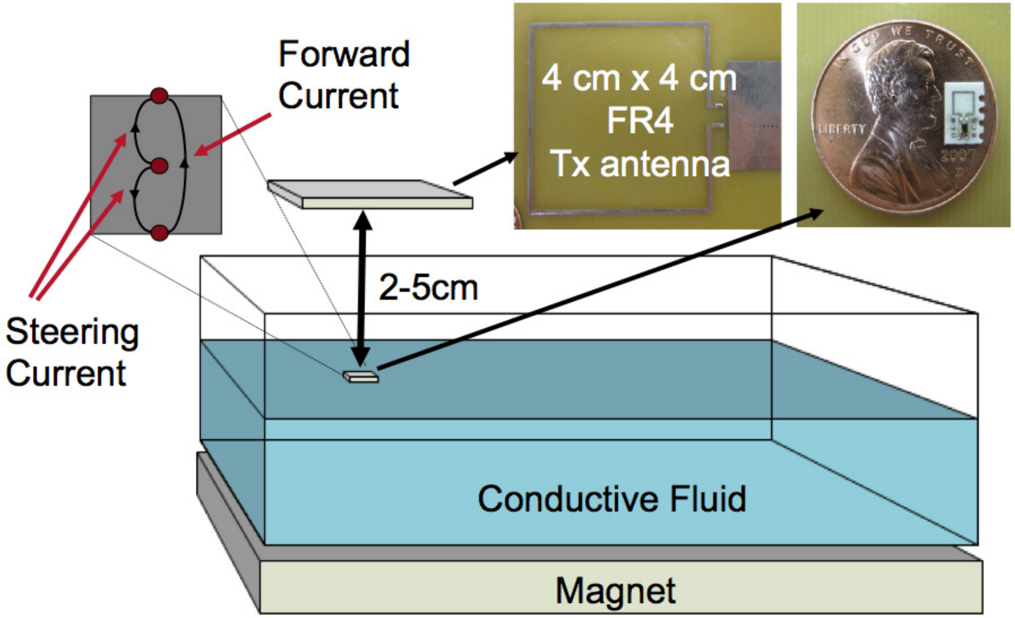
Limitation of Motion



Reference:
http://www.runyweb.com/articles/life/health/the-fda-has-approved-a-new-generation-of-israeli-videocapsule-to-check-the-small-intestine.html
Yoshihiro Kusuda, (2005) "A further step beyond wireless capsule endoscopy", Sensor Review, Vol. 25 Iss: 4, pp.259 - 260

Propulsive Force

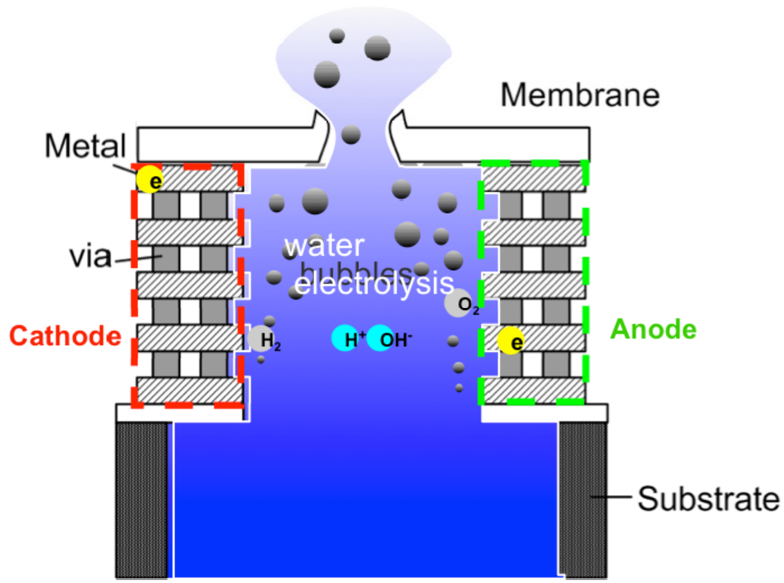
- Magnetic Actuation (Capsule Endoscopy)
- Lorenz Force (*ISSCC2012*)
- Electrolytic Bubble



Reference:
Yakovlev, A., Pivonka, D., Meng, T., Poon, A., "A mm-sized wirelessly powered and remotely controlled locomotive implantable device", *ISSCC, 2012* , vol., no., pp.302-304, 19-23 Feb. 2012.

Propulsive Force

- Magnetic Actuation (Capsule Endoscopy)
- Lorenz Force (*ISSCC2012*)
- Electrolytic Bubble (This Work)



Reference:

P.-L. Huang, P.-H. Kuo, Y.-J. Huang, H.-H. Liao, Y.-J. J. Yang, T. Wang, Y.-H. Wang, S.-S. Lu, "A Controlled-Release Drug Delivery System on a Chip Using Electrolysis", *IEEE Trans. Industrial Electronics,* vol.59, no.3, pp.1578-1587, March 2012.

Locomotive Implantable SoC

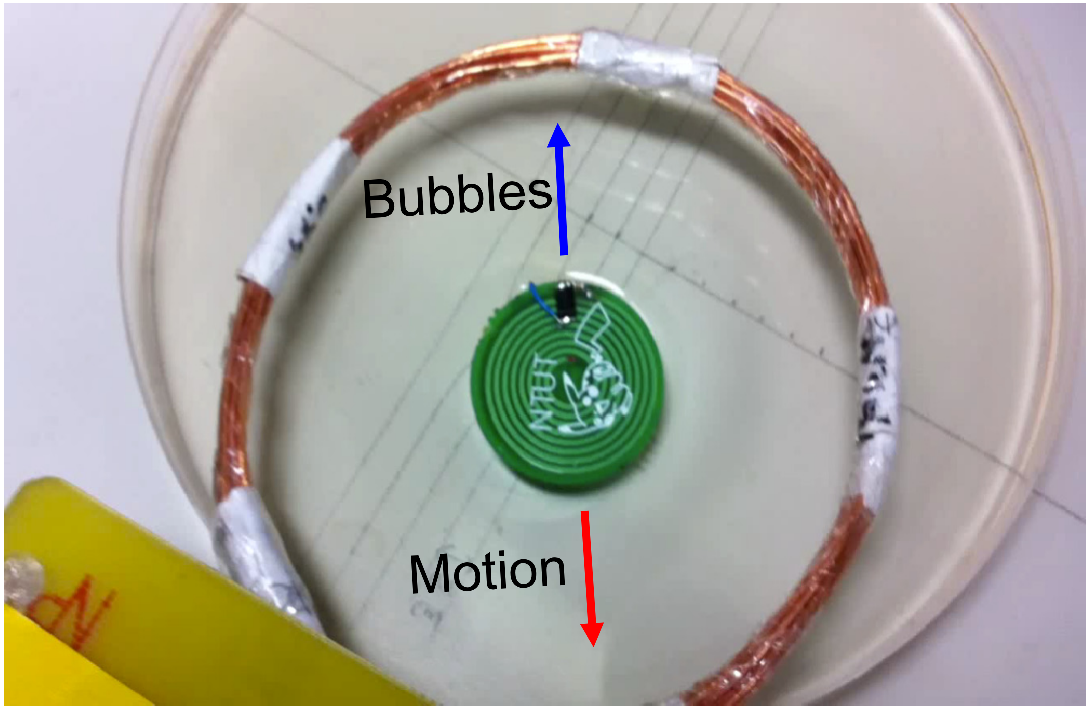
Design Consideration:

- Implantable
- Wireless Powered
- Remotely Control
- Cruising Ability

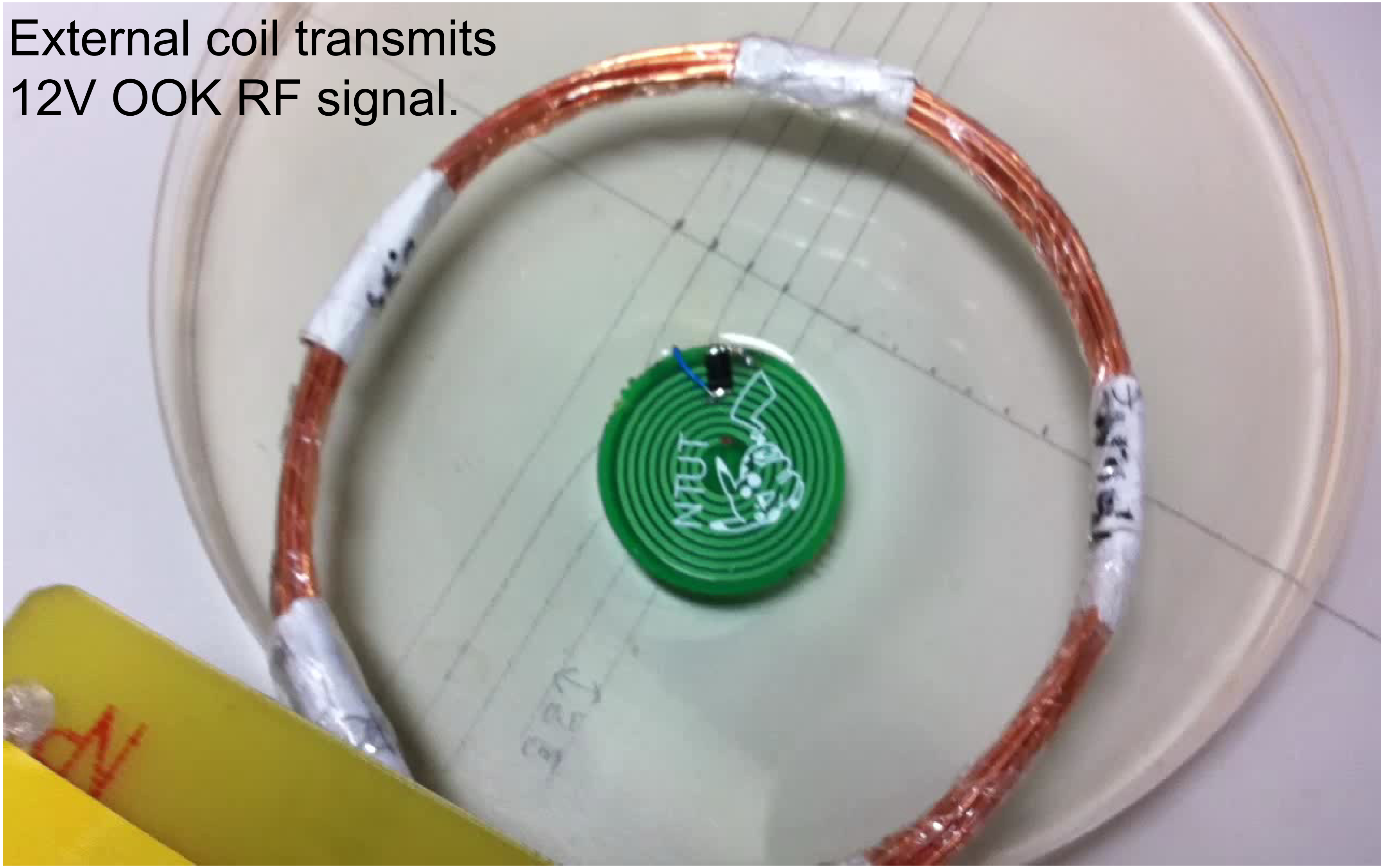
Motion Test on PCB

PCB RX (back side)

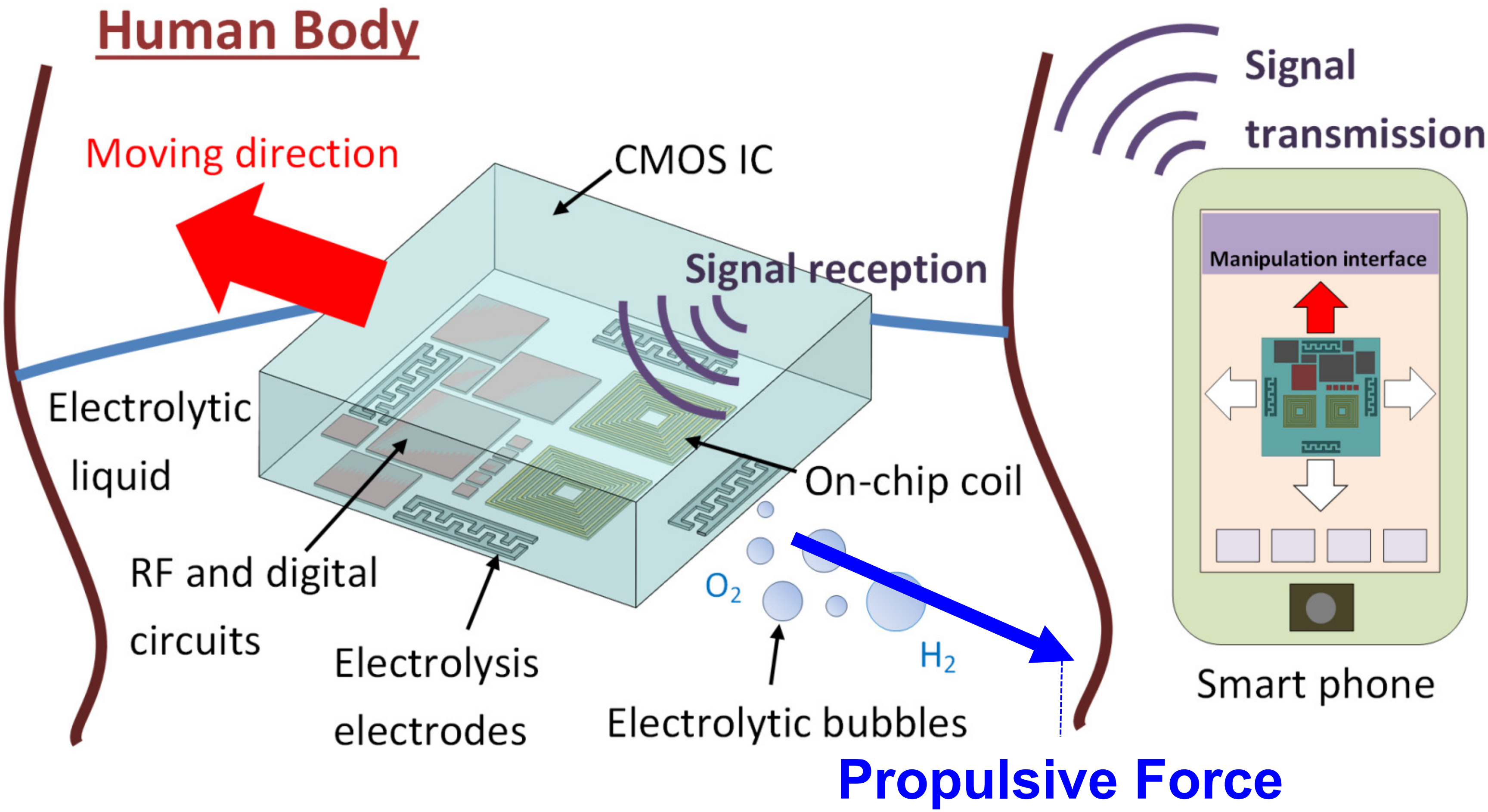
External coil transmits 12V OOK RF signal.



Motion Test on PCB



Wireless Powered, Remotely Controlled Locomotive Chip



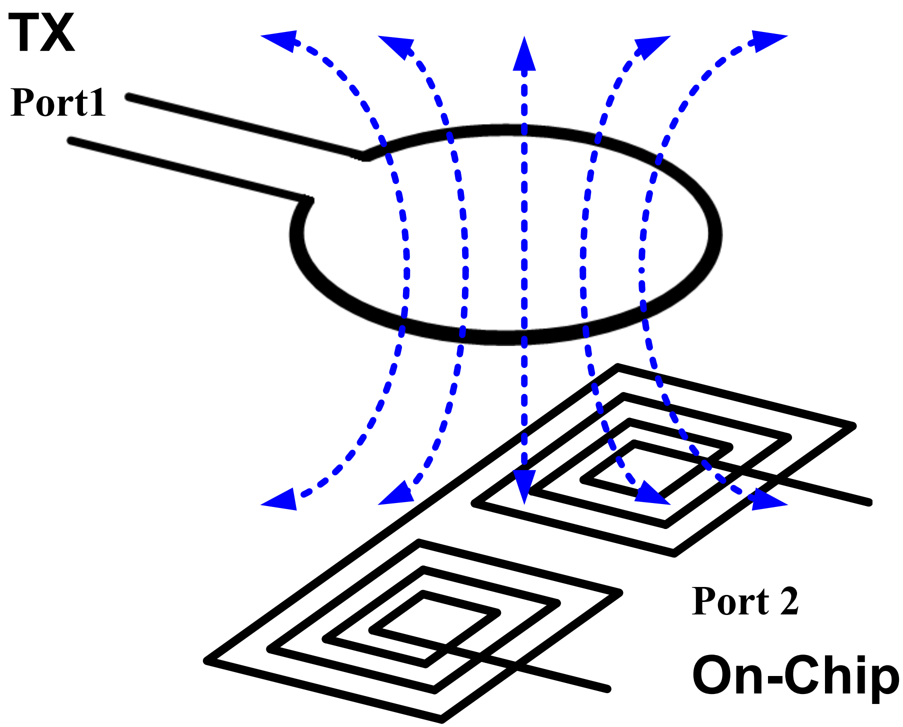
On-Chip Electrolysis

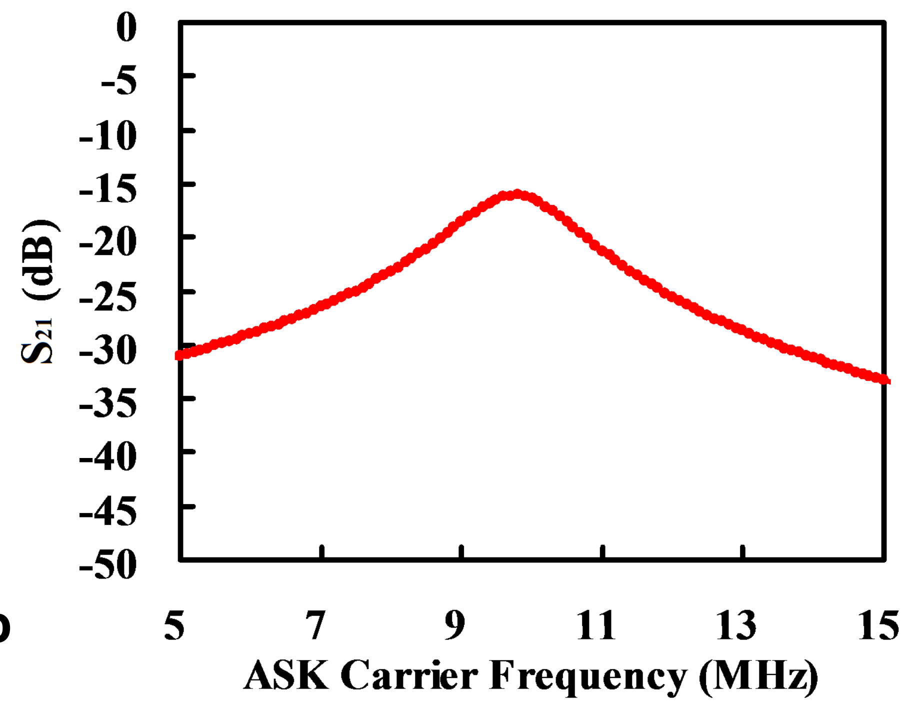
Year	Method	Membrane Materials
1999 [1]	electrochemical	Au
2005 [2]	electrothermal	Au or Ti/Pt

1) J. T. Santini Jr *et al.*, "A controlled-release microchip," *Nature*, Vol. 397, 1999, pp.335-338

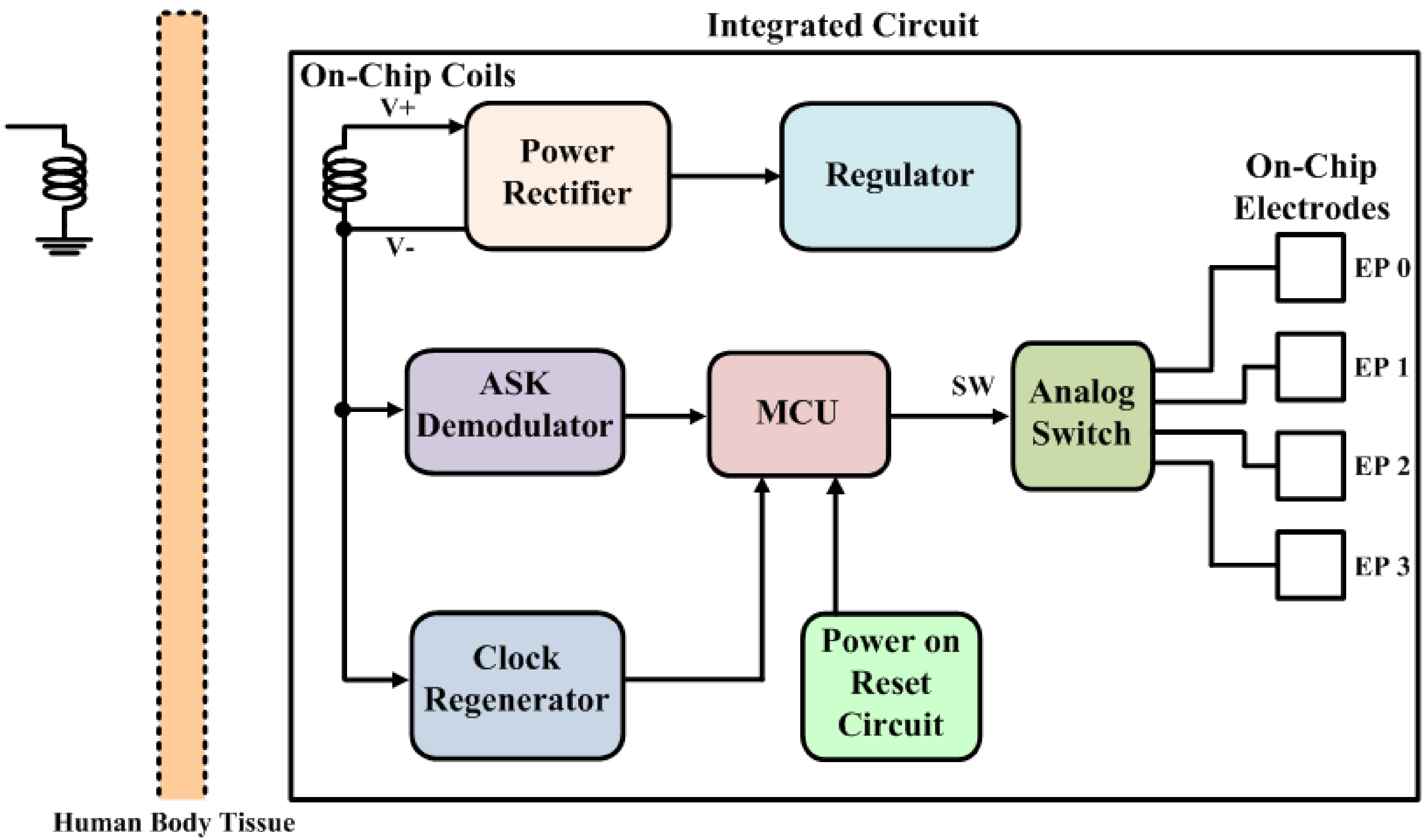
2) J. M. Maloney *et al.*, "Electrothermally activated microchips for implantable drug delivery and biosensing," *Journal of Controlled Release*, Vol. 109, 2005, pp. 244-255

RF Coupling Simulation

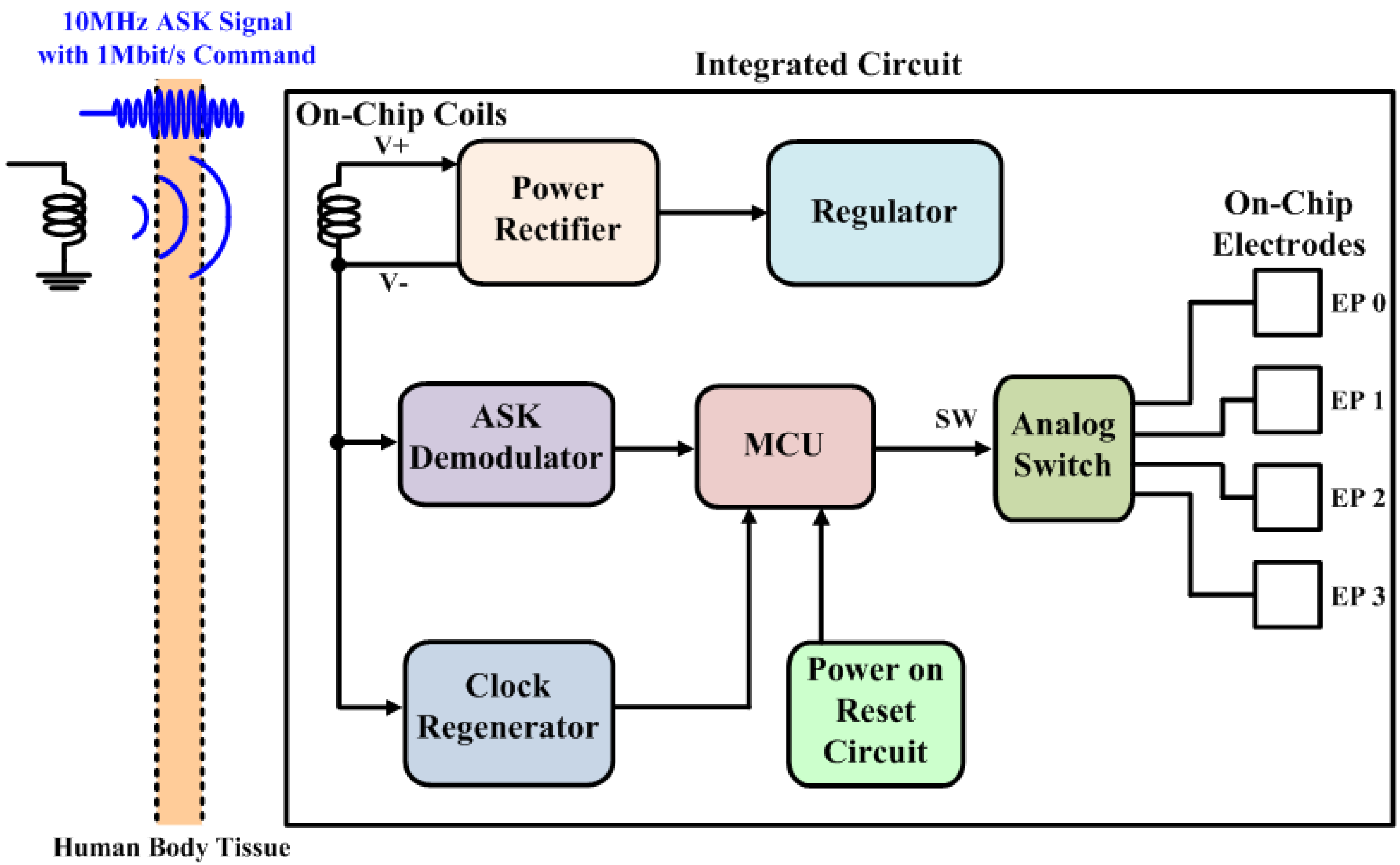




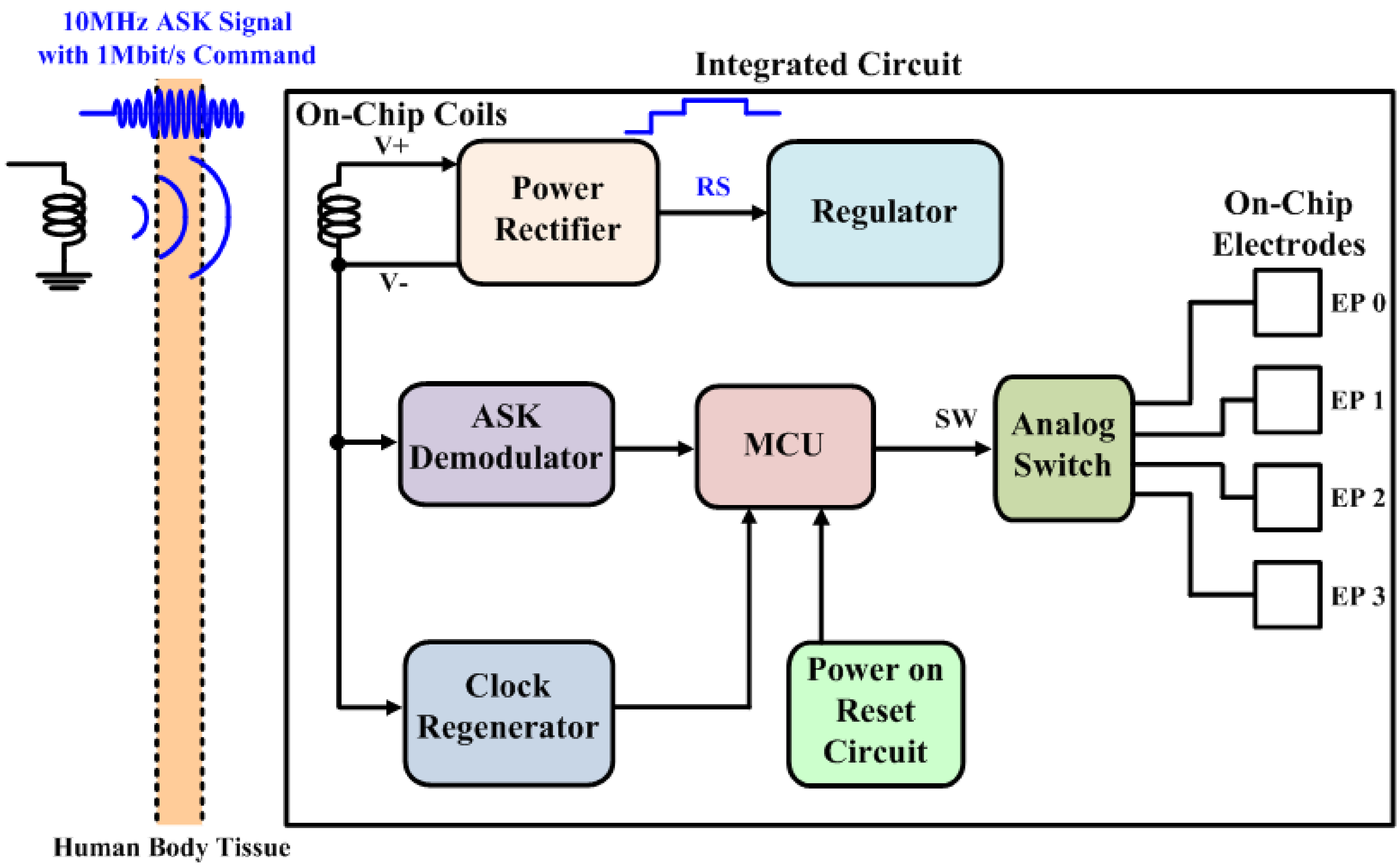
Schematic of the Remotely Controlled Locomotive CMOS IC



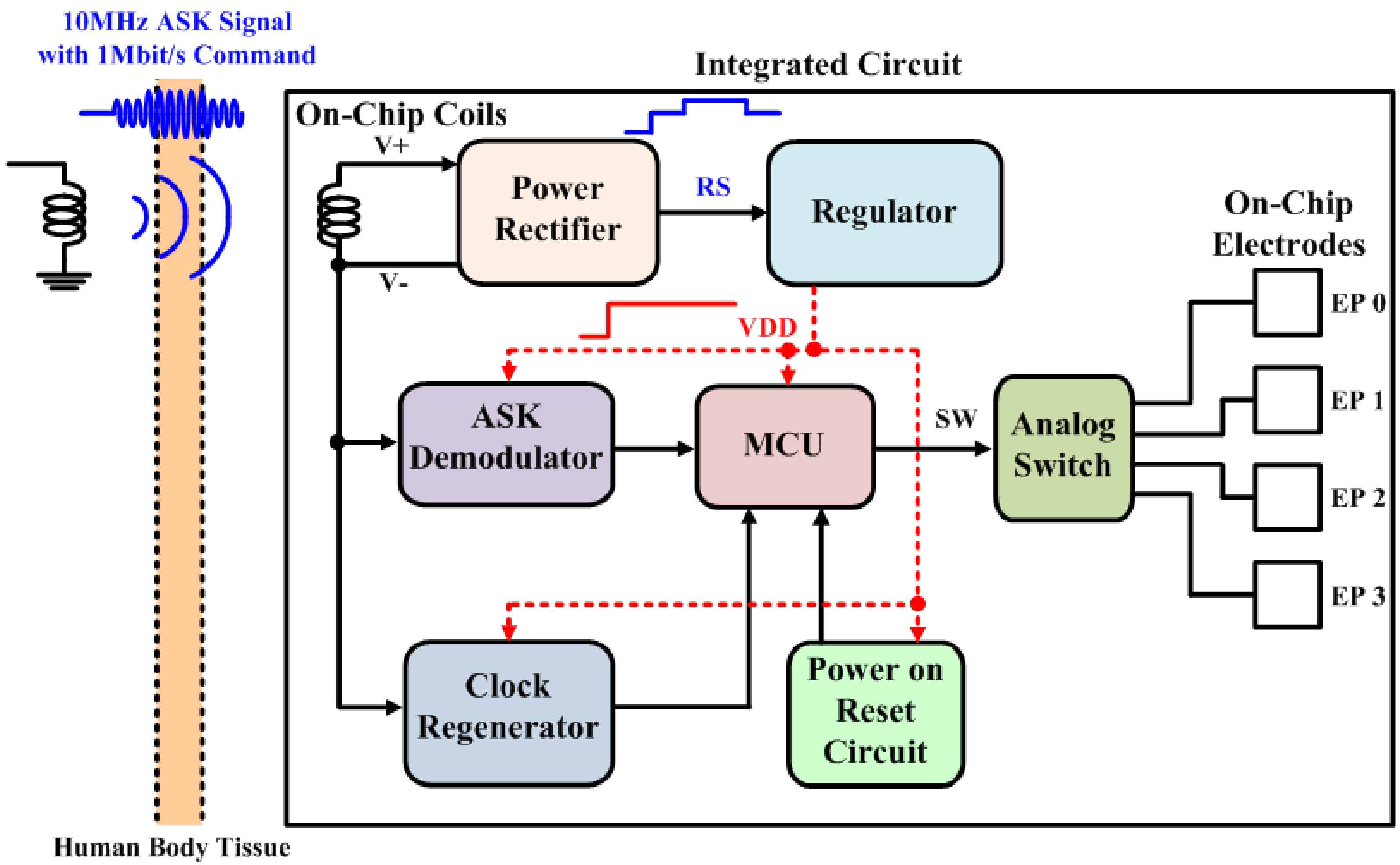
Schematic of the Remotely Controlled Locomotive CMOS IC



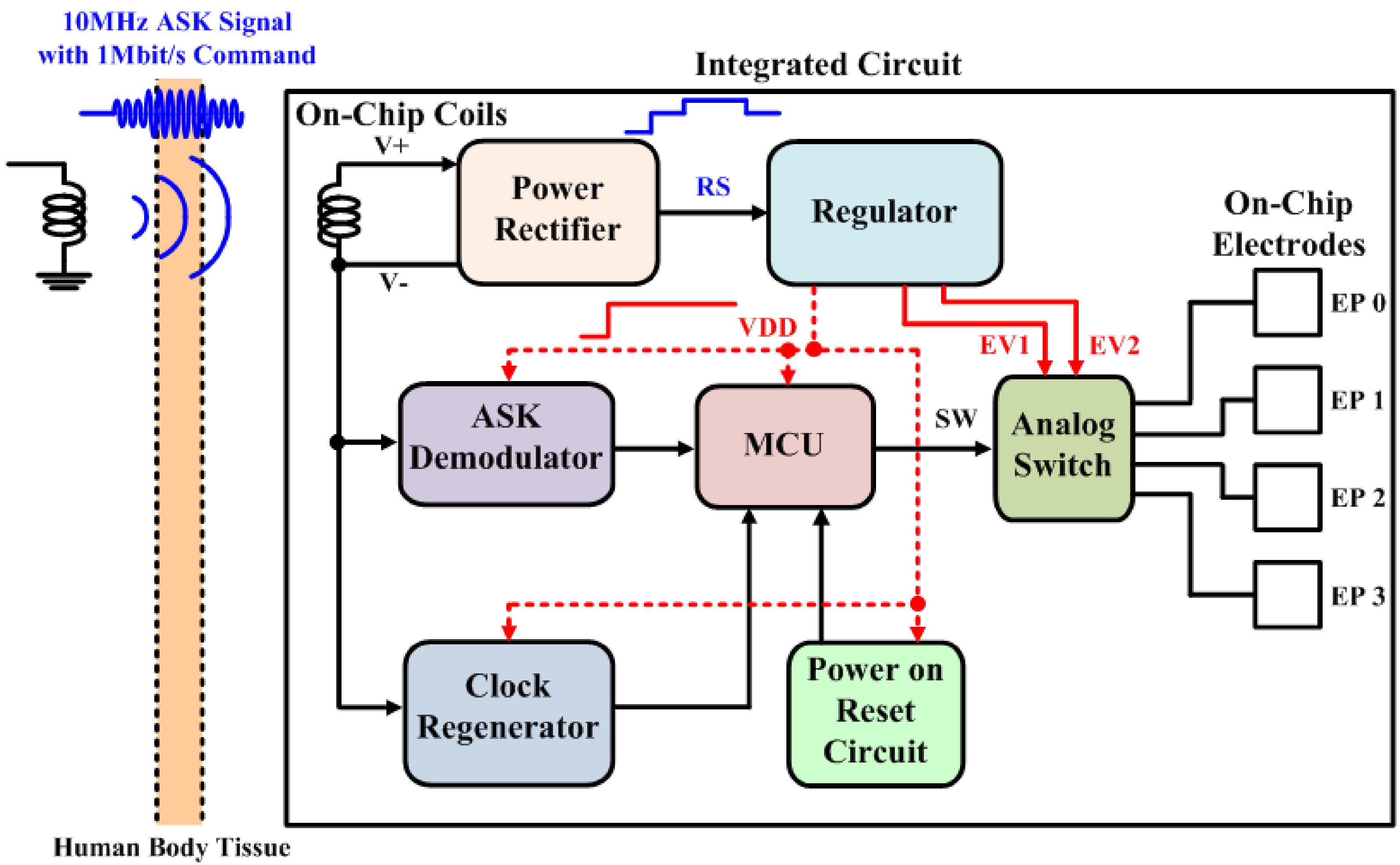
Schematic of the Remotely Controlled Locomotive CMOS IC



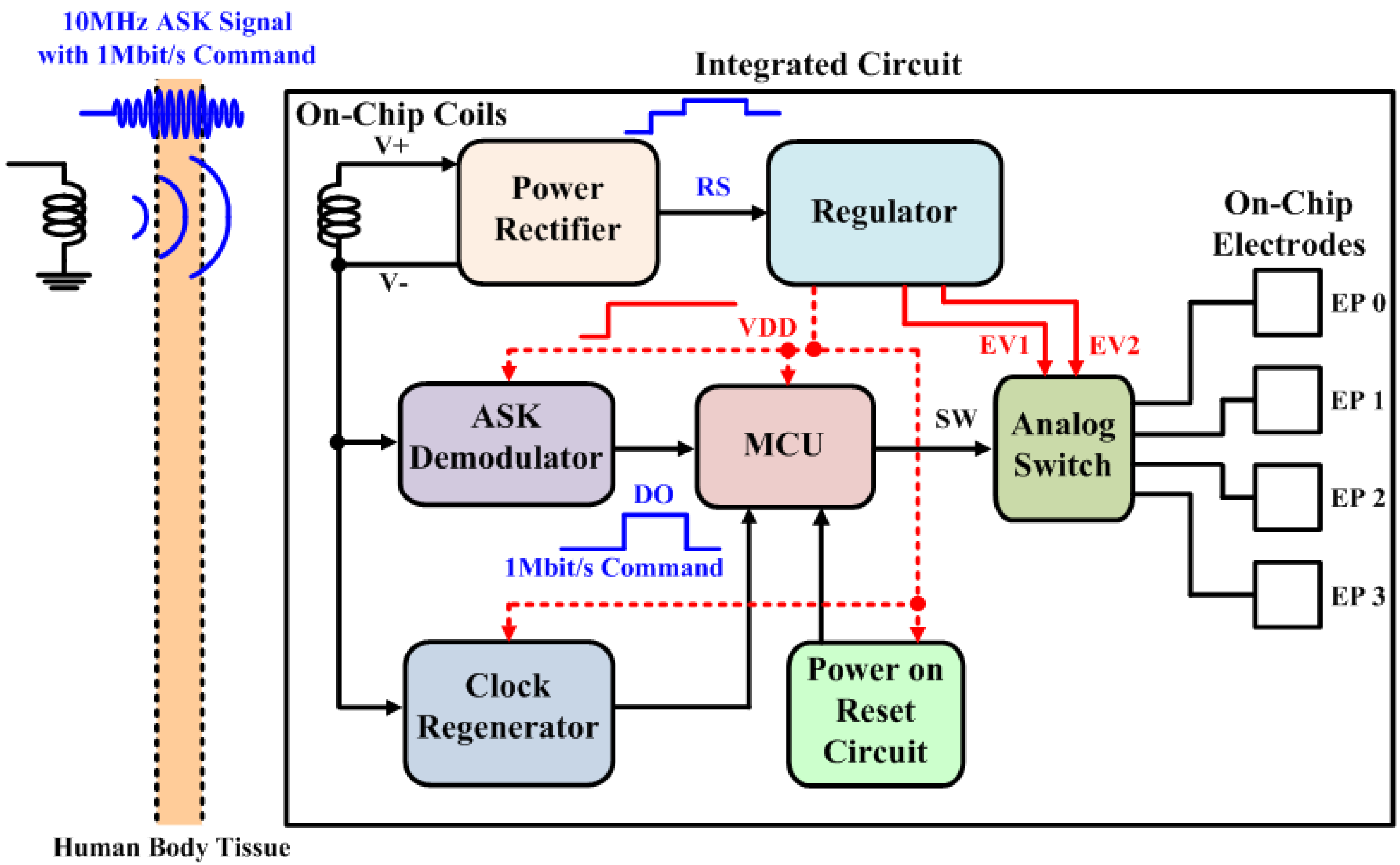
Schematic of the Remotely Controlled Locomotive CMOS IC



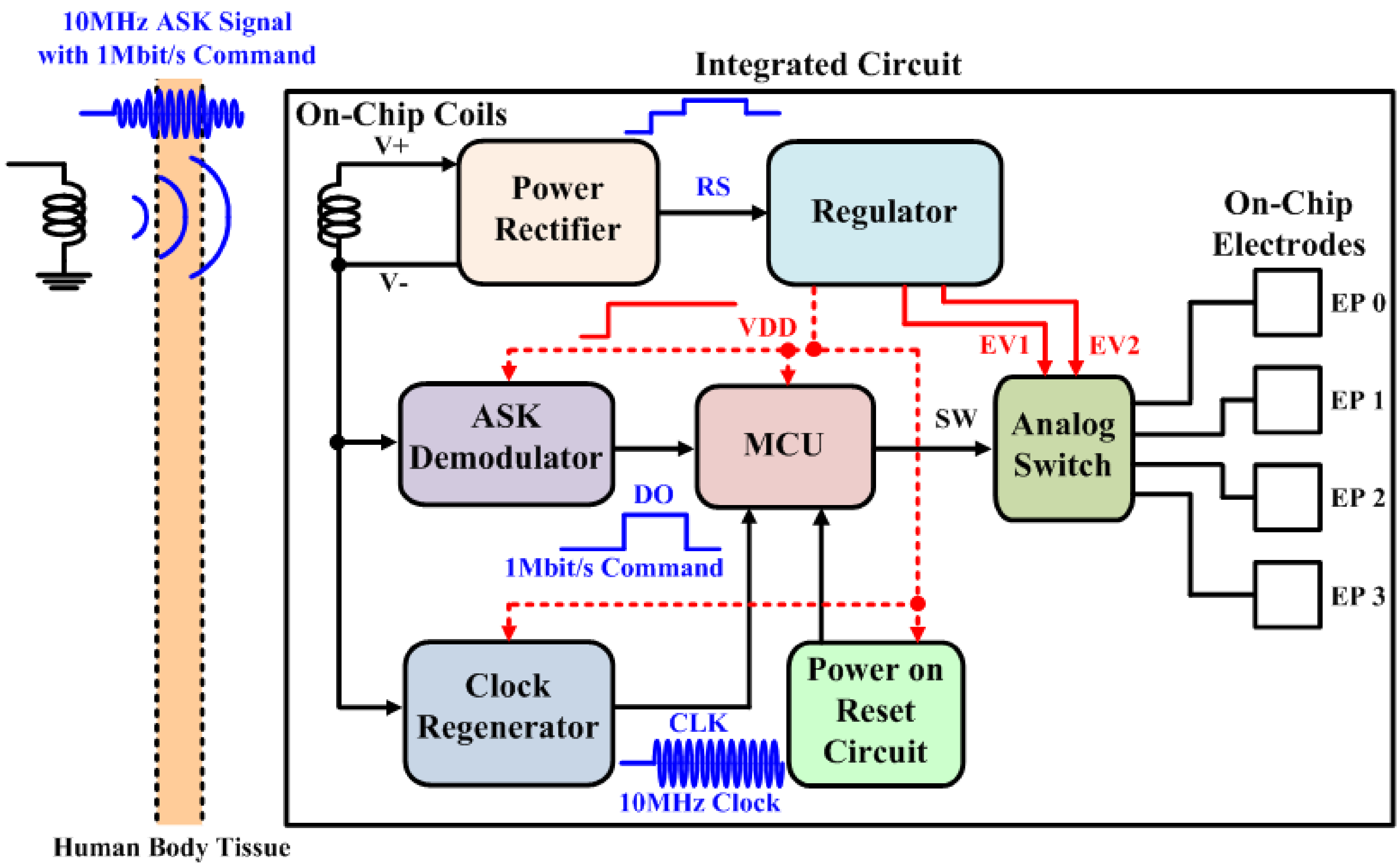
Schematic of the Remotely Controlled Locomotive CMOS IC



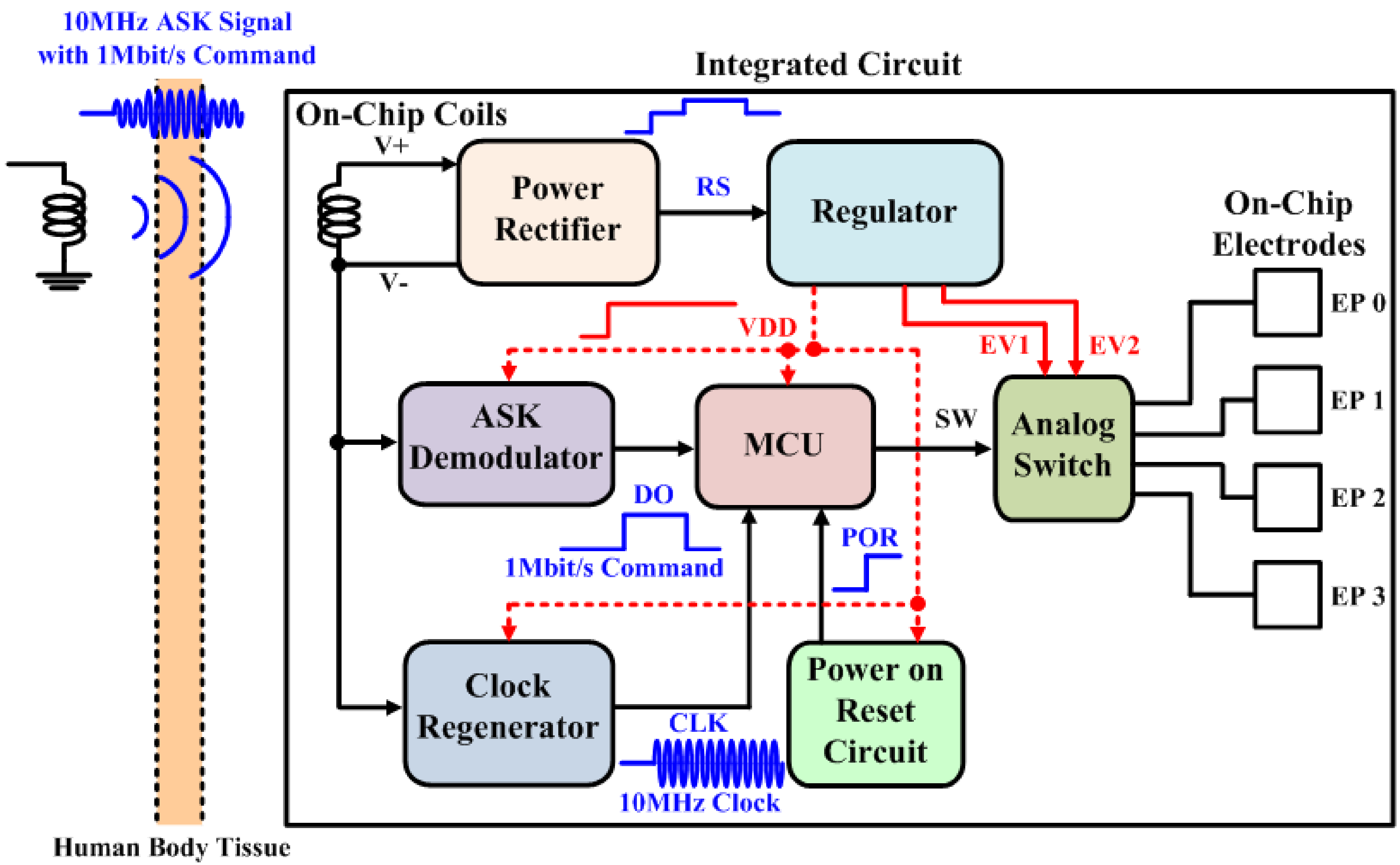
Schematic of the Remotely Controlled Locomotive CMOS IC



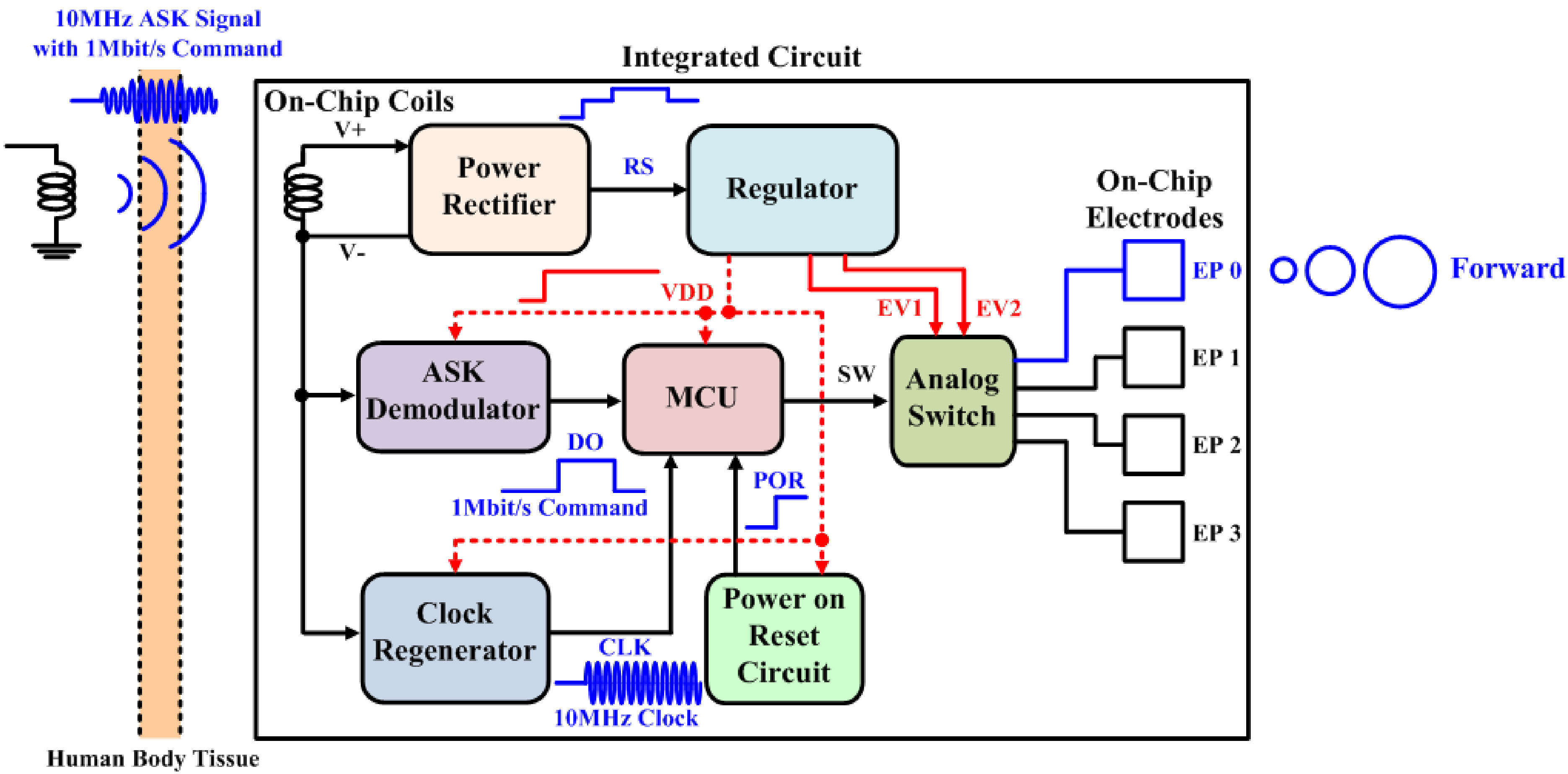
Schematic of the Remotely Controlled Locomotive CMOS IC



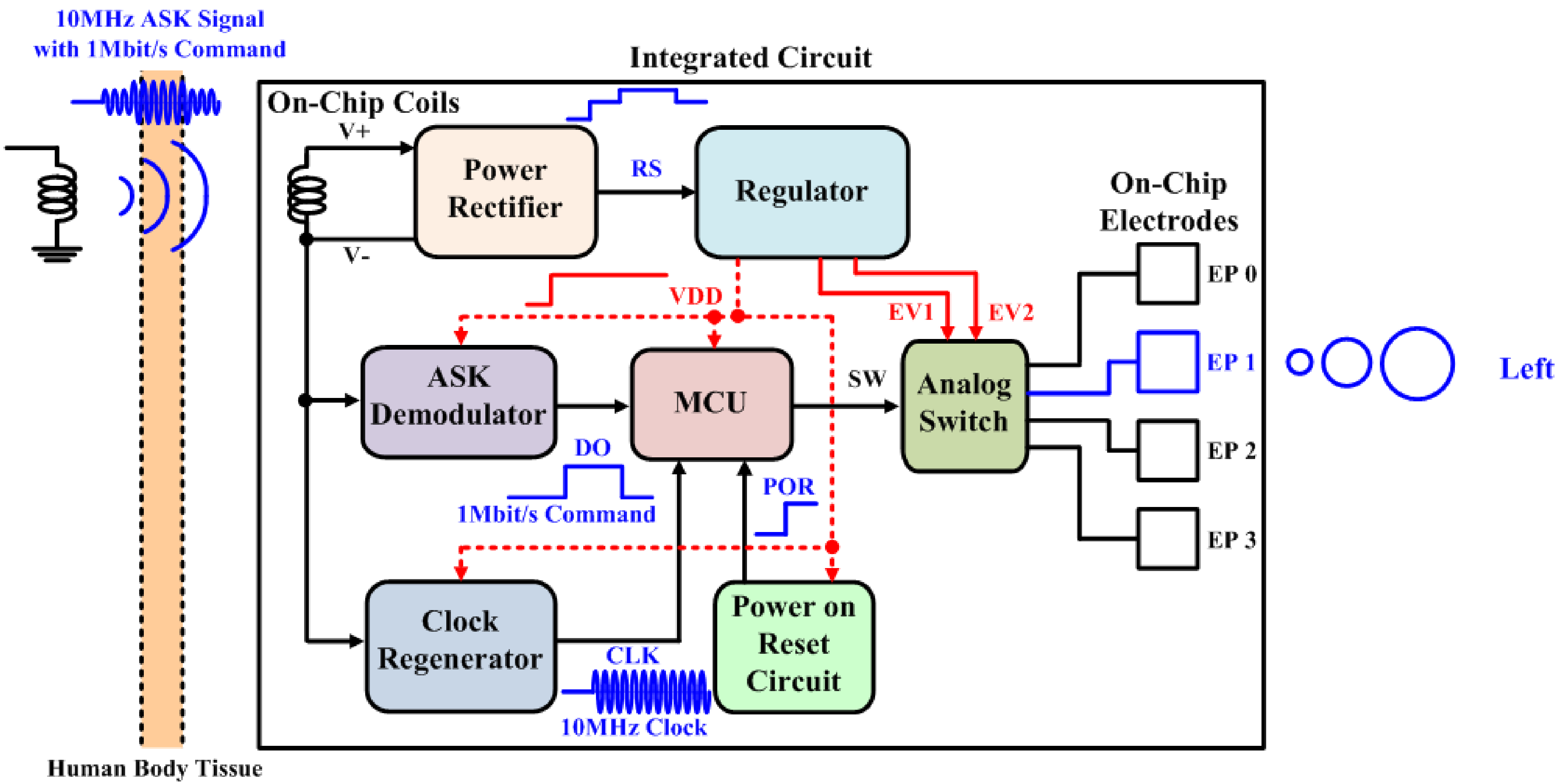
Schematic of the Remotely Controlled Locomotive CMOS IC



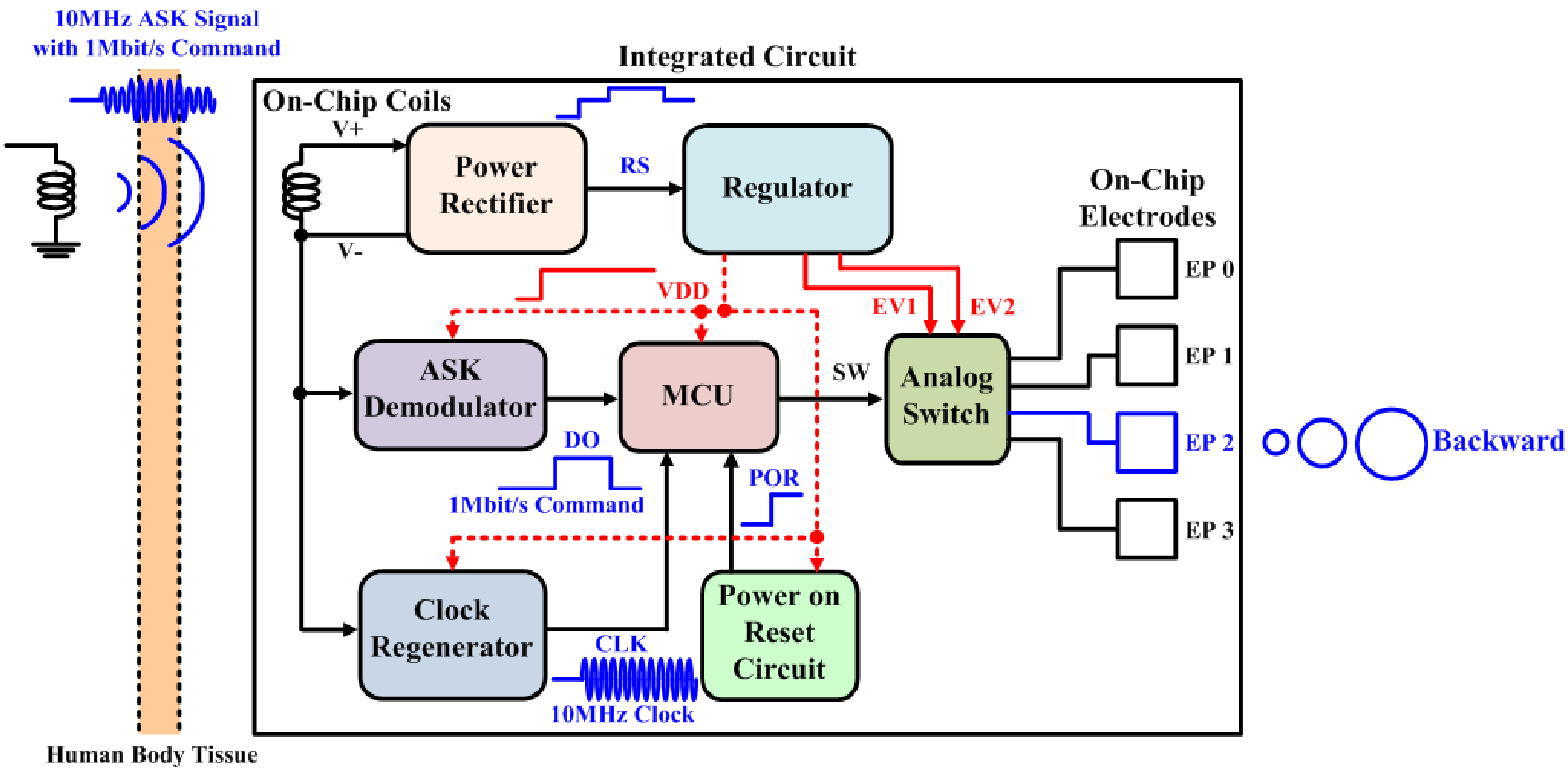
Schematic of the Remotely Controlled Locomotive CMOS IC



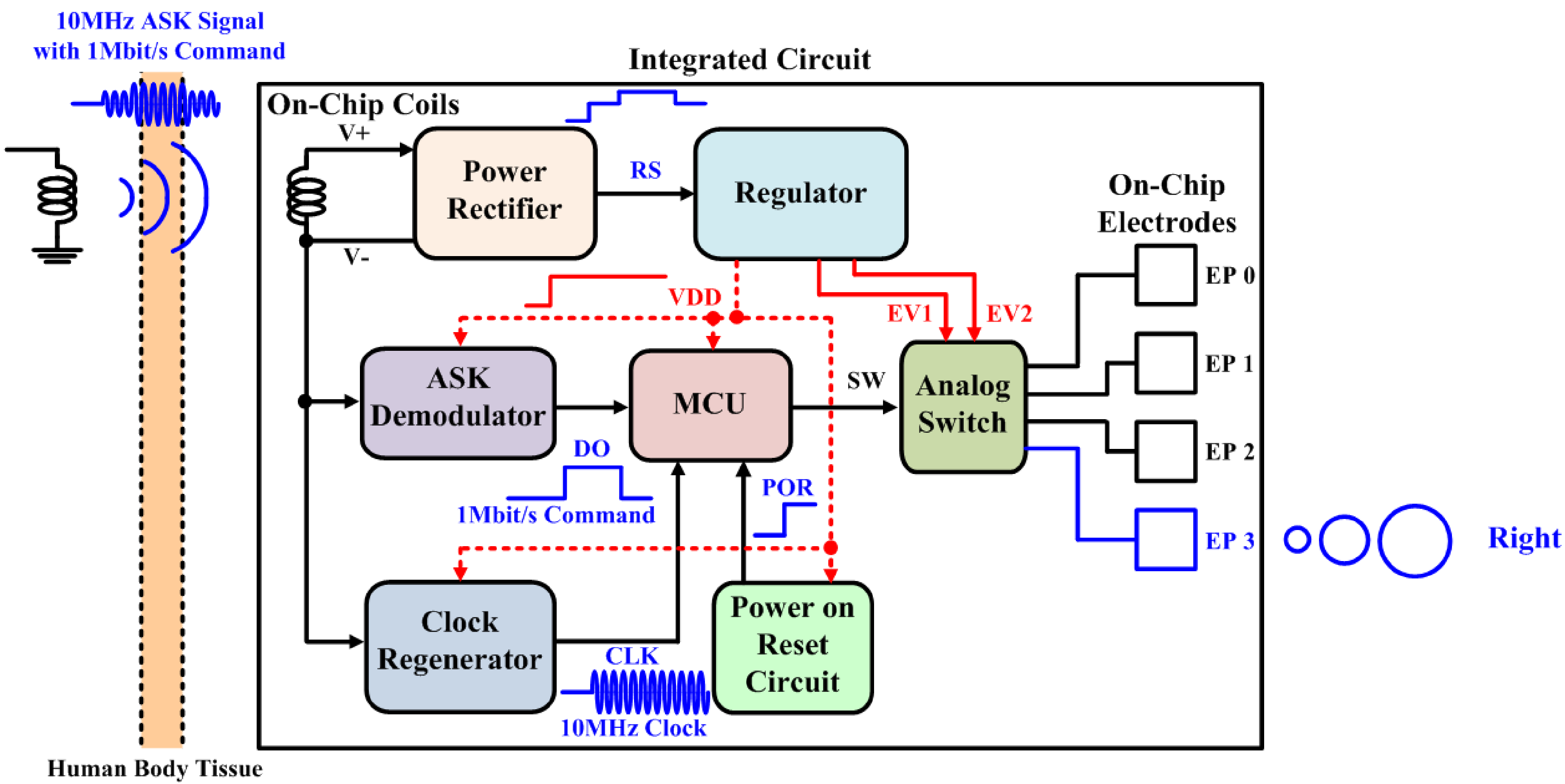
Schematic of the Remotely Controlled Locomotive CMOS IC



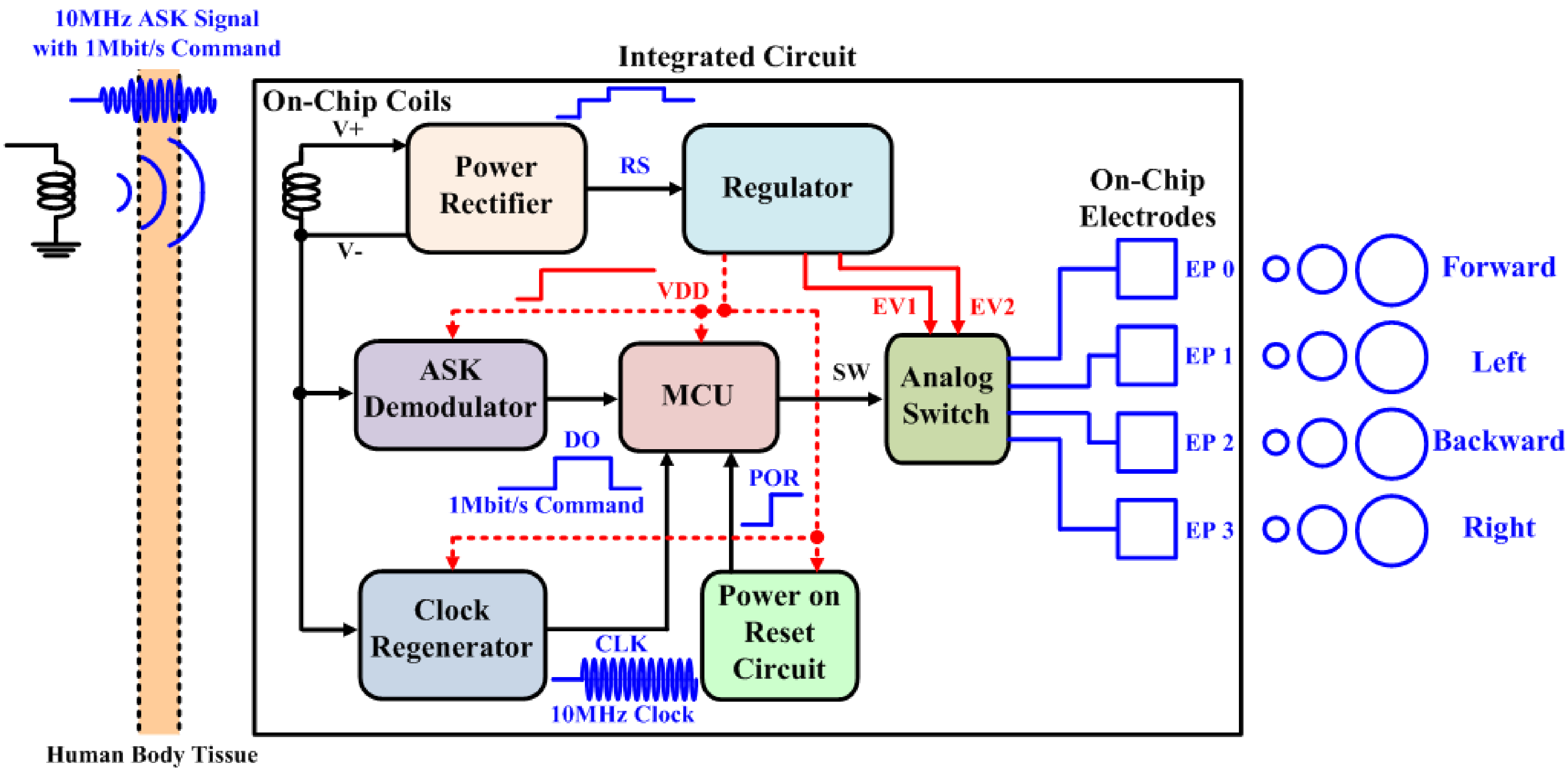
Schematic of the Remotely Controlled Locomotive CMOS IC



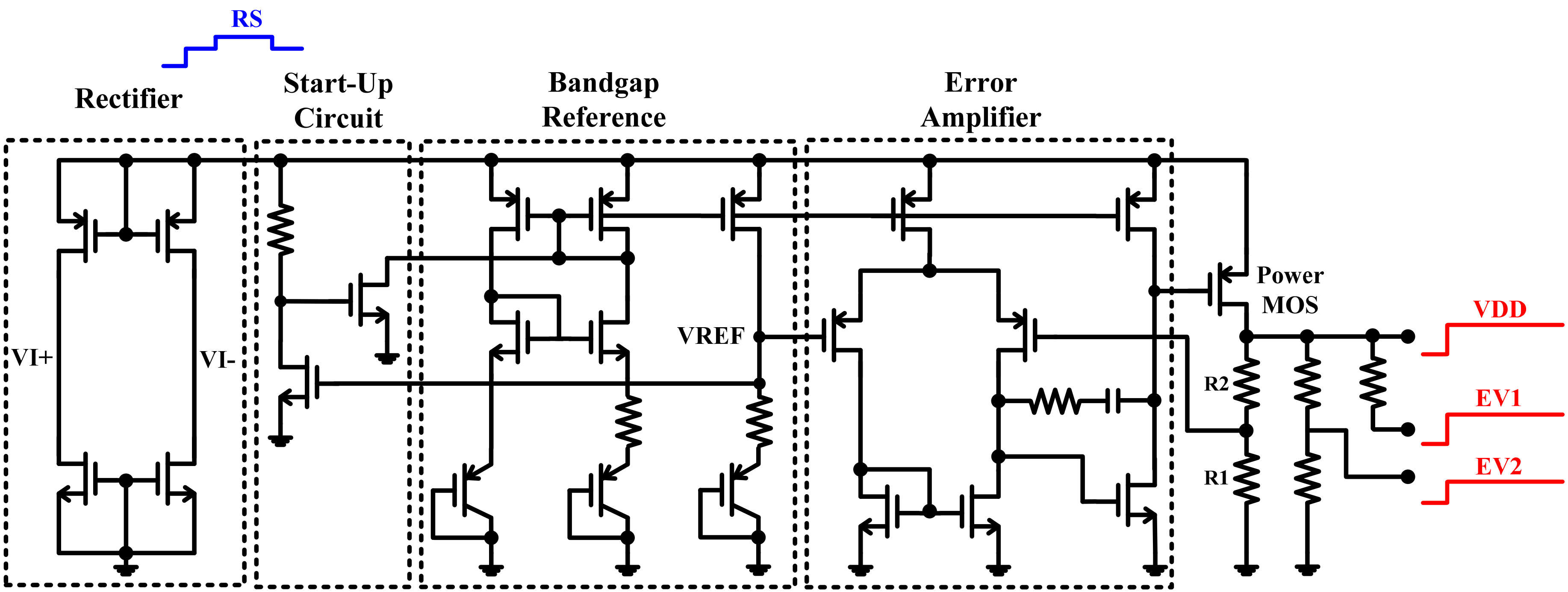
Schematic of the Remotely Controlled Locomotive CMOS IC



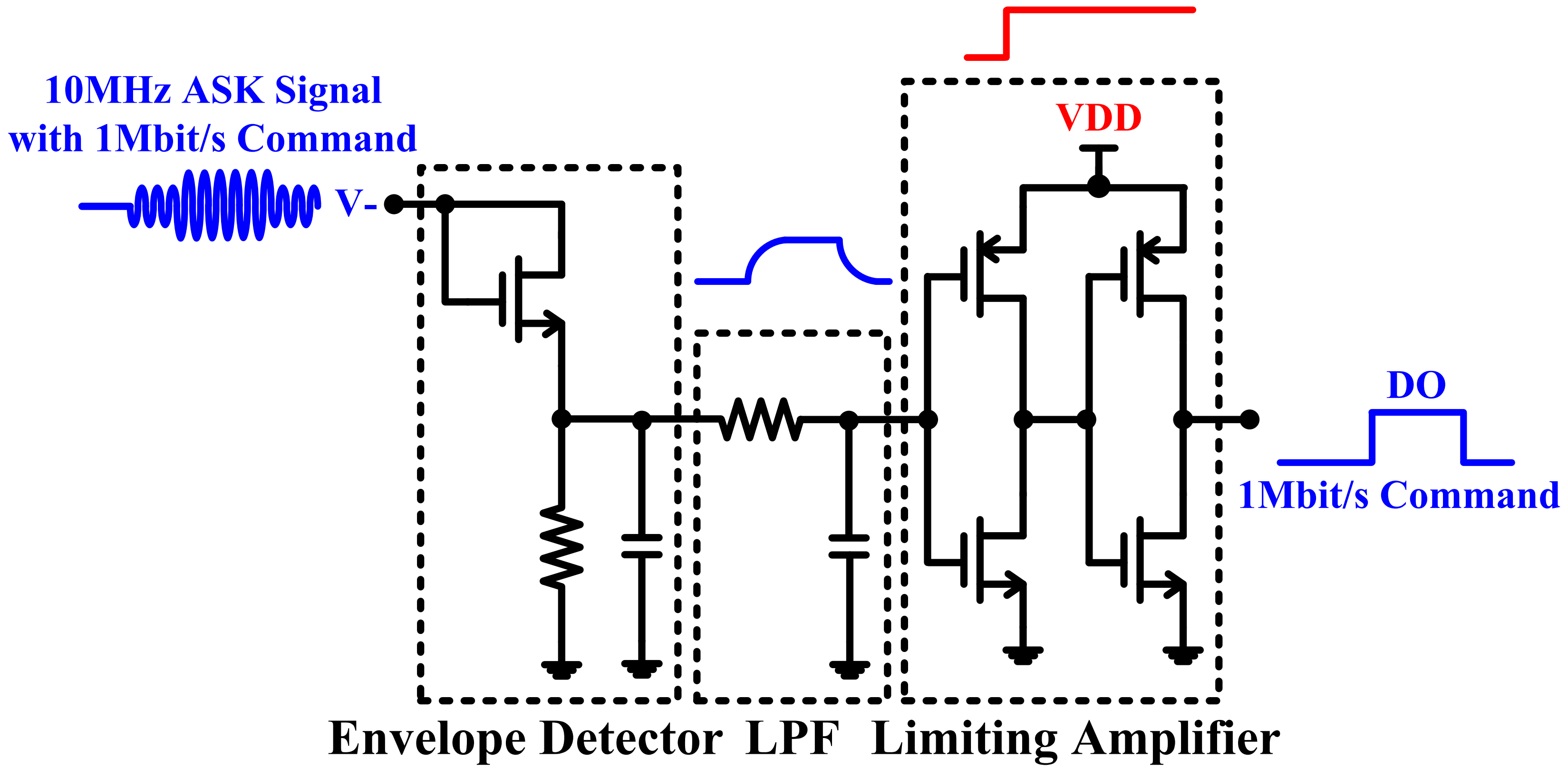
Schematic of the Remotely Controlled Locomotive CMOS IC



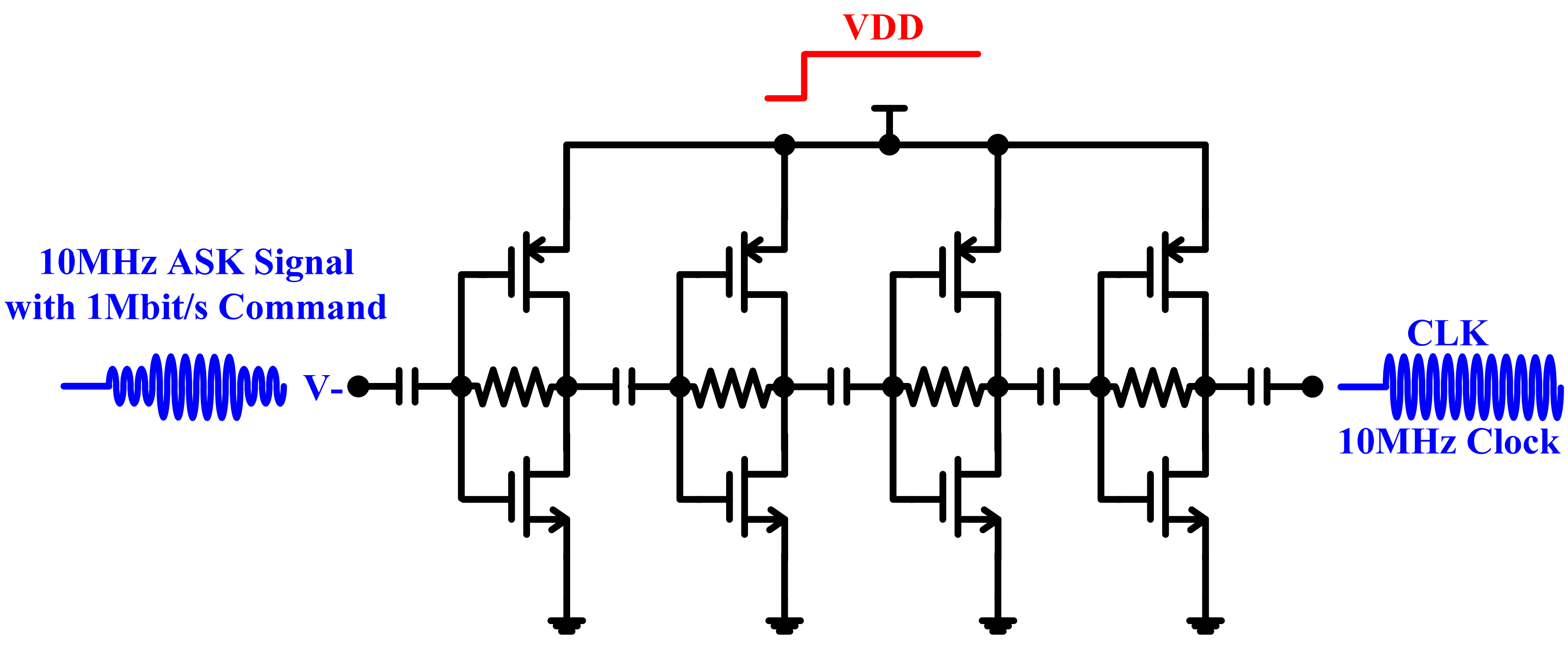
RF-DC


RS
Rectifier
Start-Up Circuit
Bandgap Reference
Error Amplifier
VI+
VI-
VREF
Power MOS
VDD
EV1
EV2
R2
R1

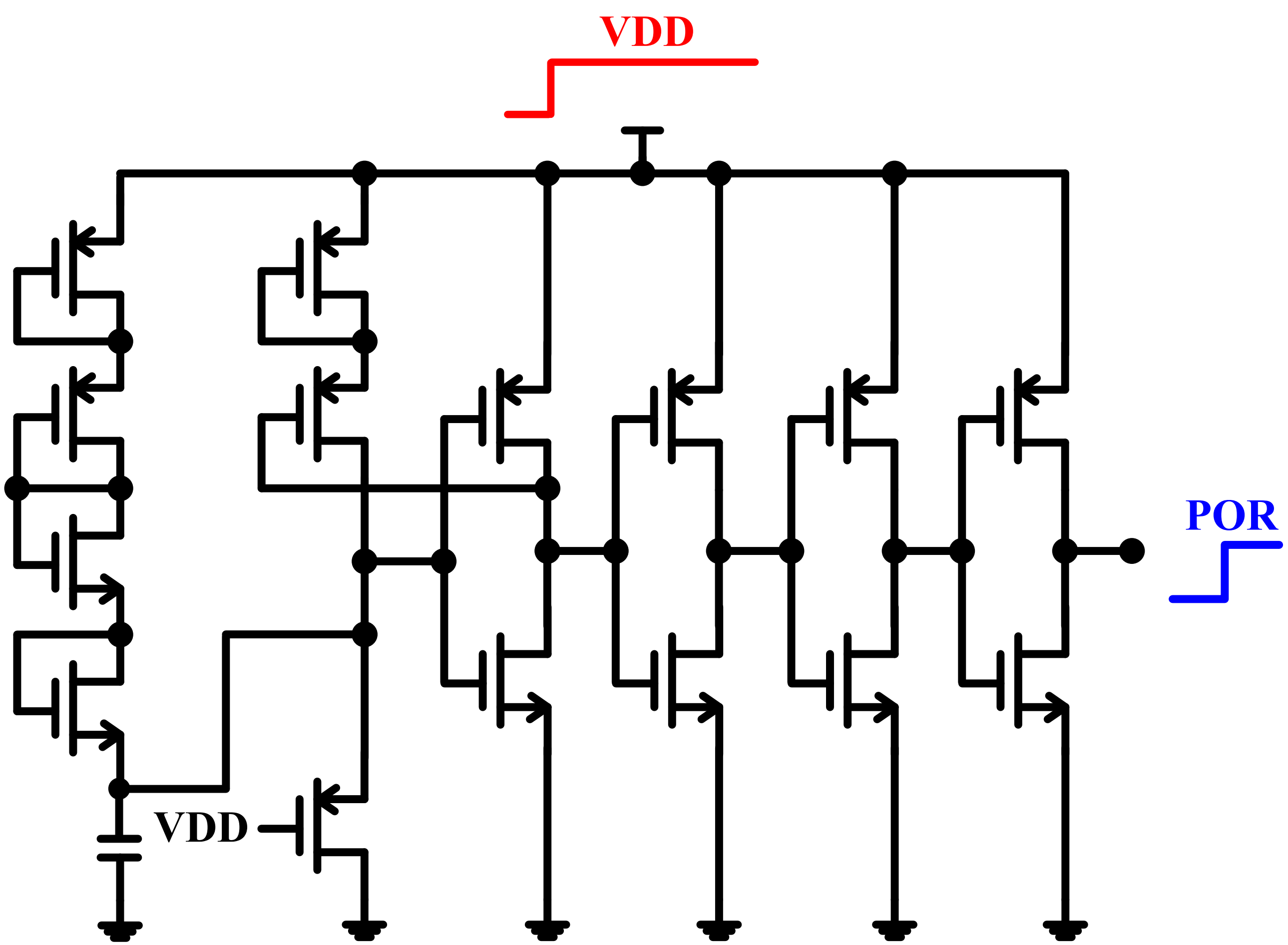
ASK Demodulator



Clock Regenerator



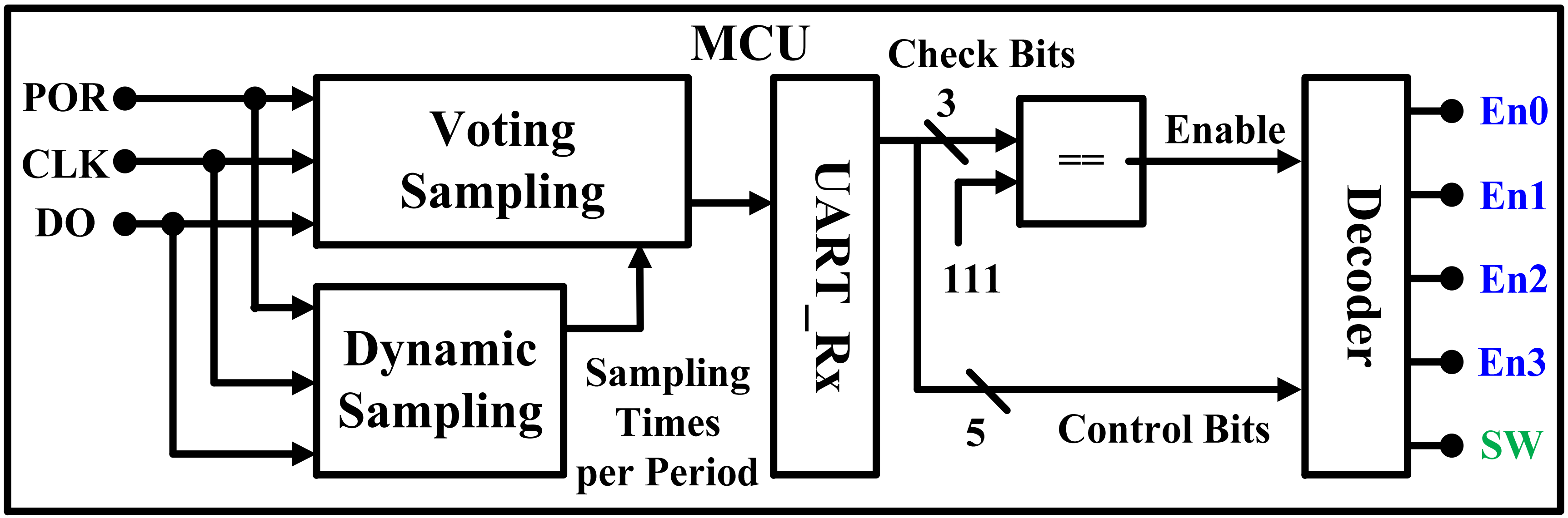
Power On Reset Circuit



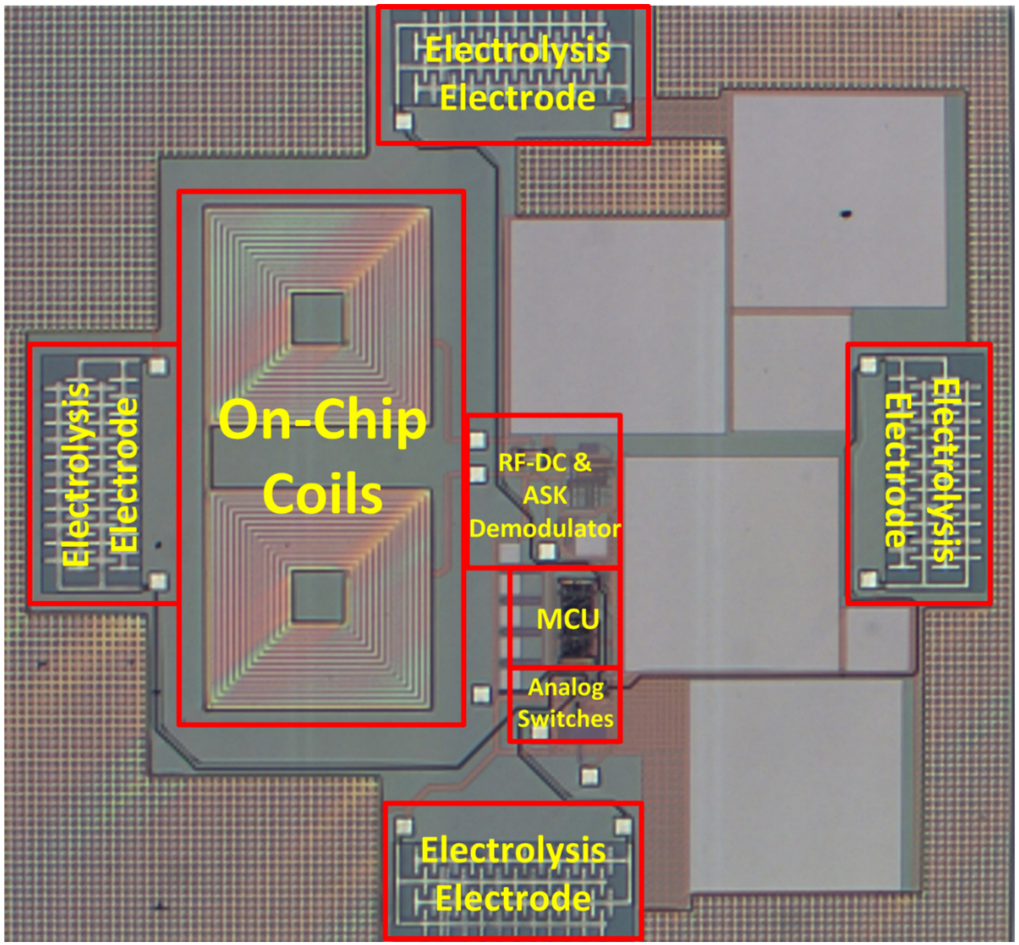
MCU

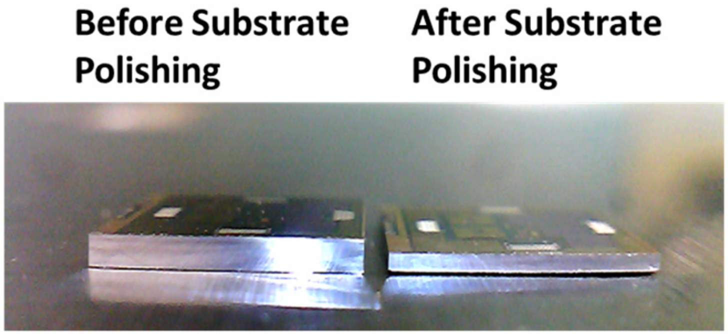
Four Directions

Two Speeds

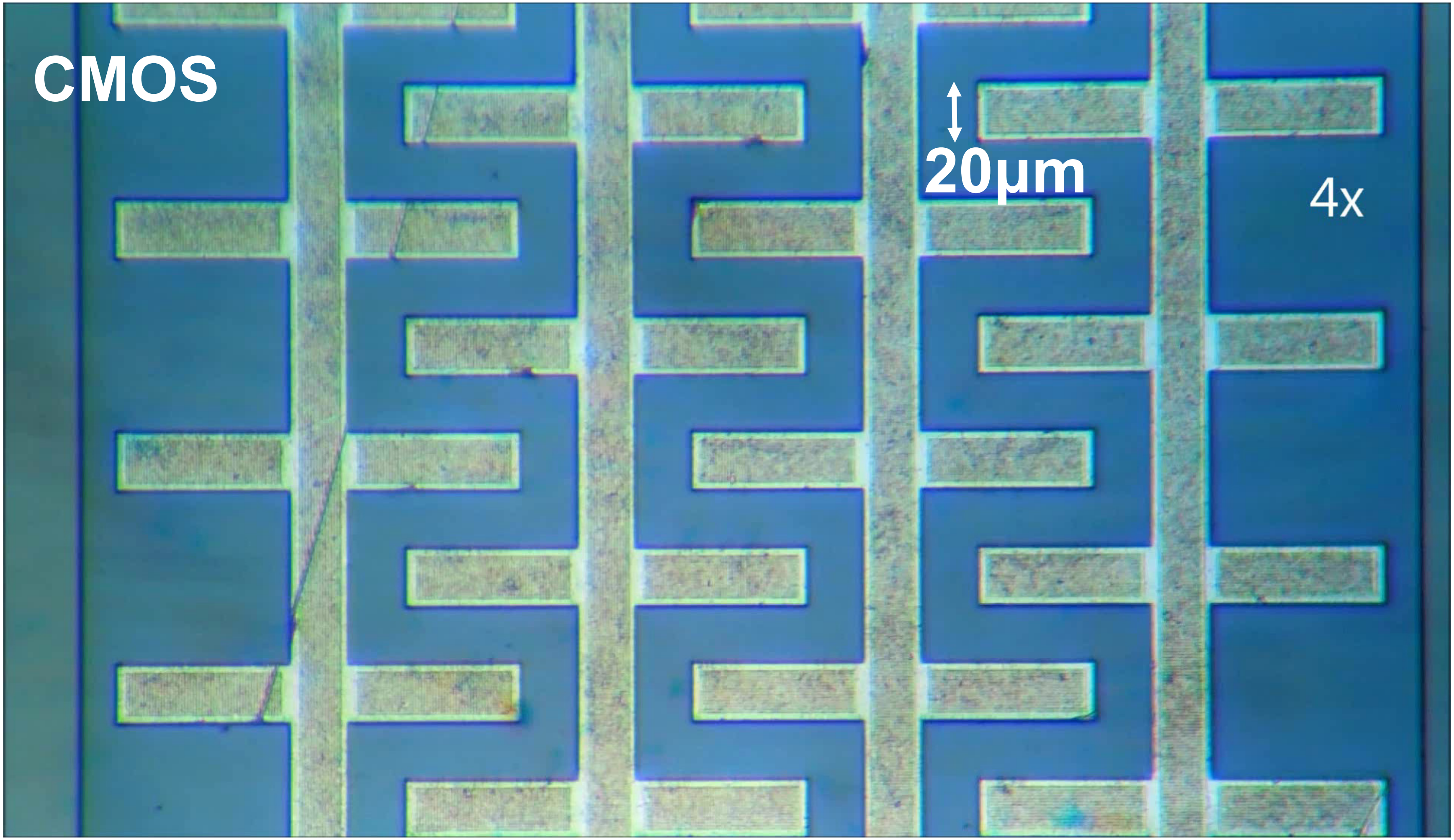


Chip Photo


Electrolysis Electrode
Electrolysis Electrode
On-Chip Coils
RF-DC & ASK Demodulator
MCU
Analog Switches
Electrolysis Electrode
Electrolysis Electrode

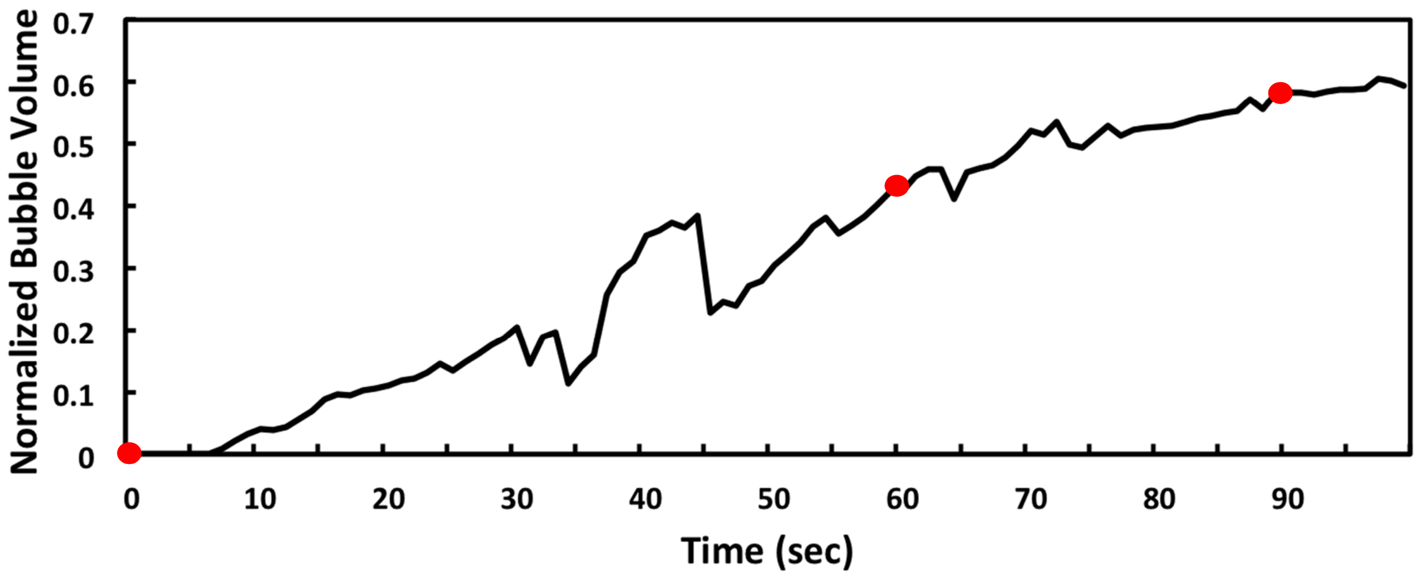

Before Substrate Polishing
After Substrate Polishing

Electrolytic Bubble



Normalized Bubble Volume

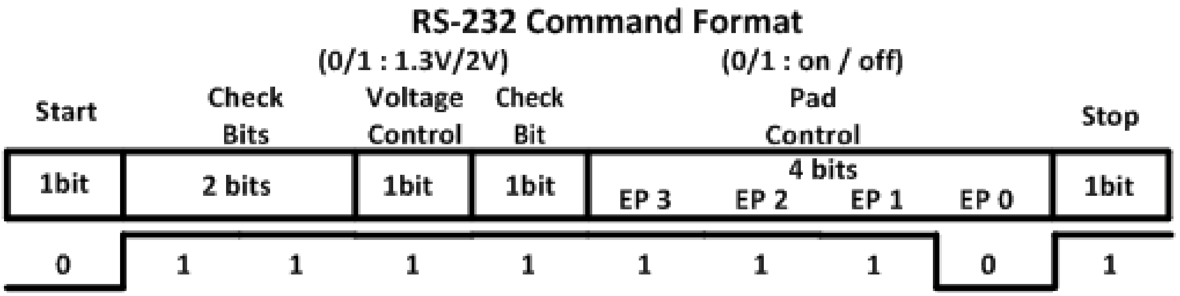
$$\textbf{Normalized Volume} = \frac{\mathbf{A}}{\mathbf{B}}$$

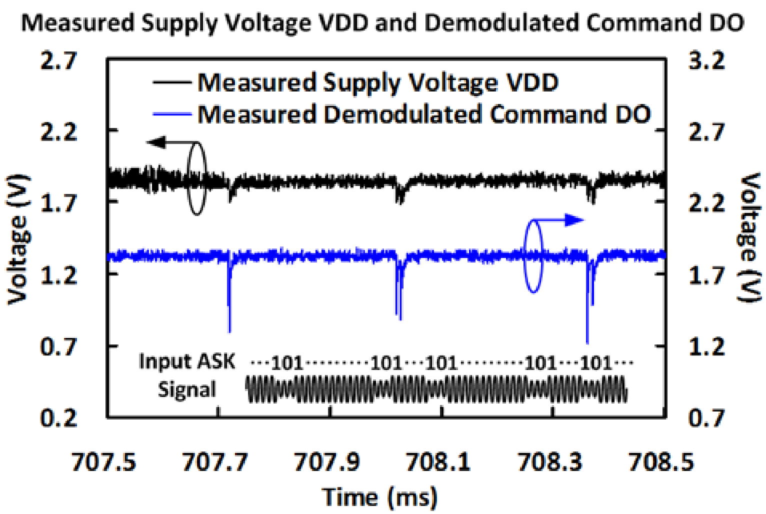


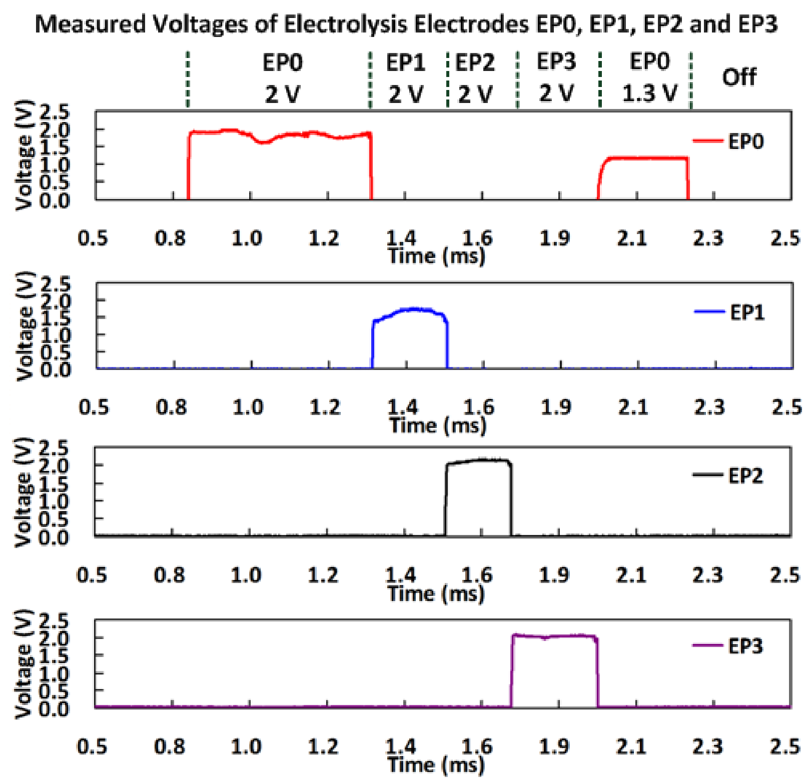
The bubbles volume is ~20nL, much smaller than harmless volume of 30μL in circulation.

T. J. Toung, et. al, "Volume of air in a lethal venous air embolism," *Anesthesiology*, vol. 94, no. 2, pp. 360–361, Feb. 2001.

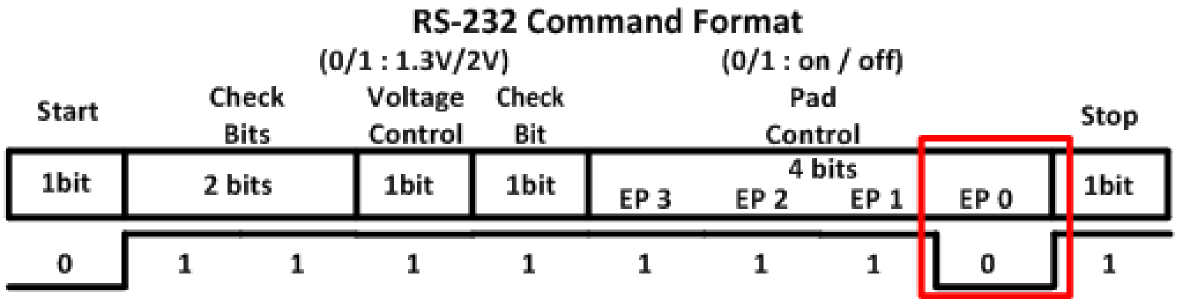
Demodulation

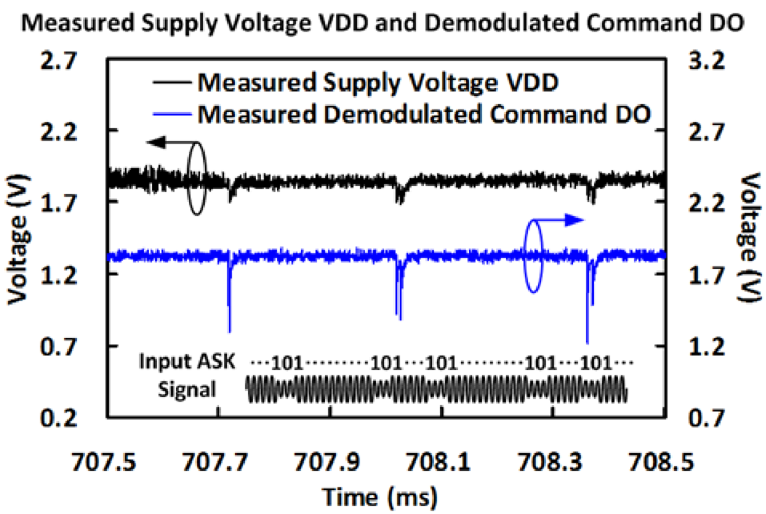


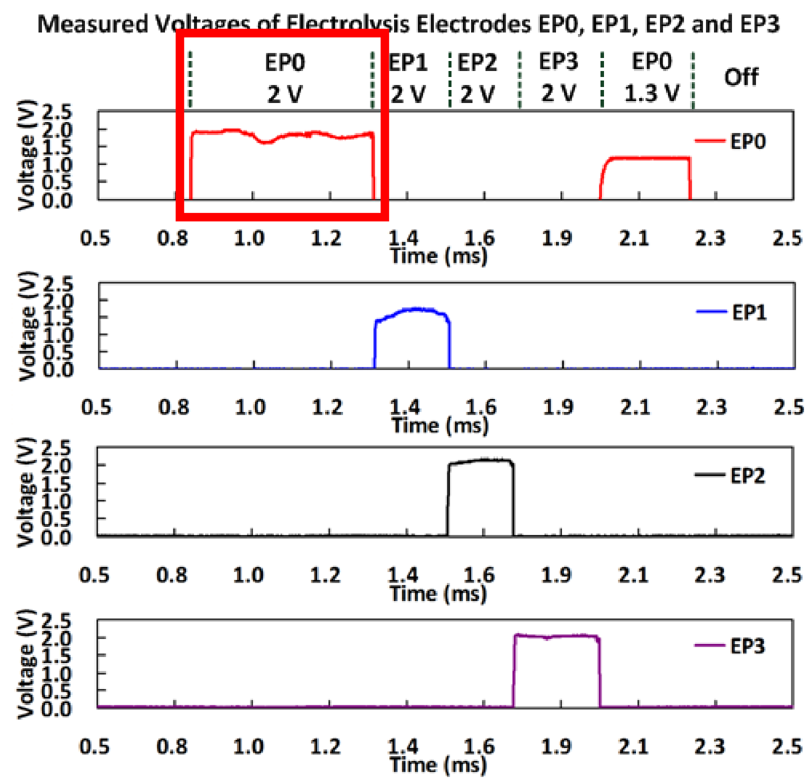




Demodulation

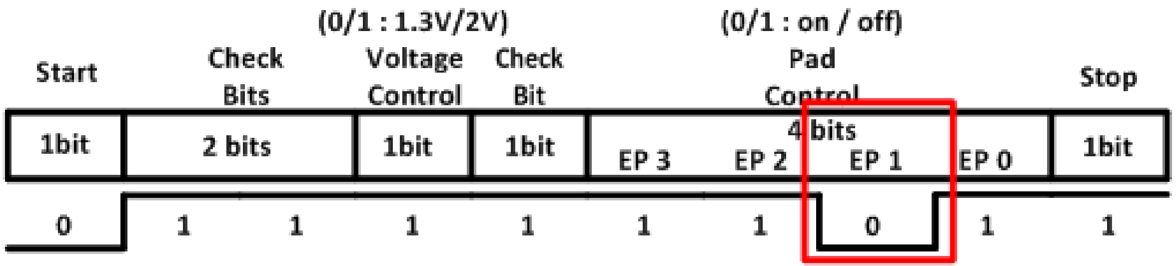




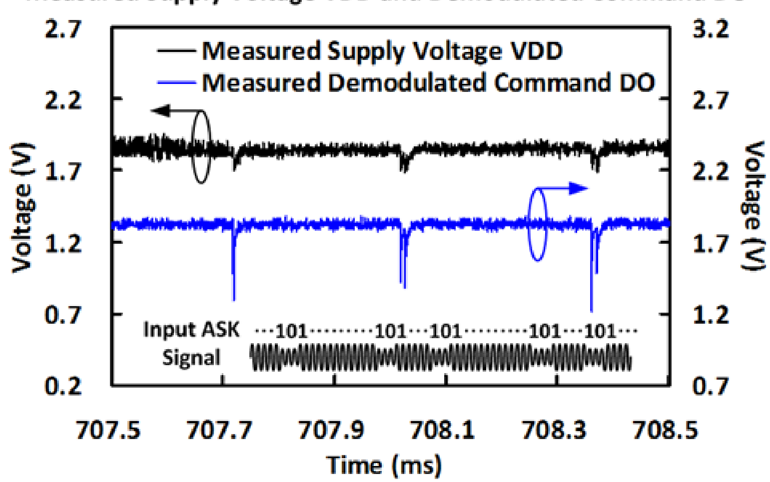


Demodulation

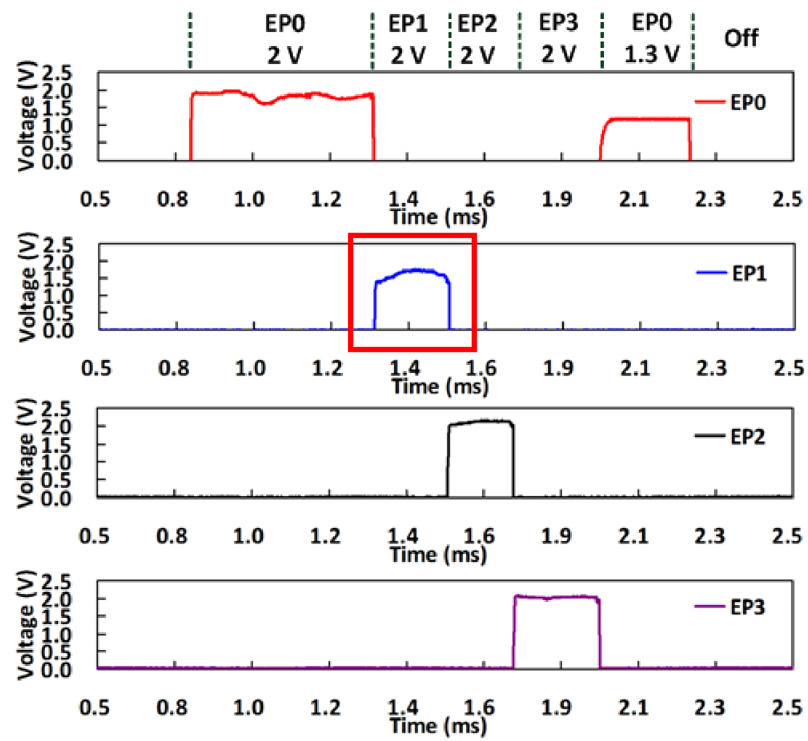
RS-232 Command Format



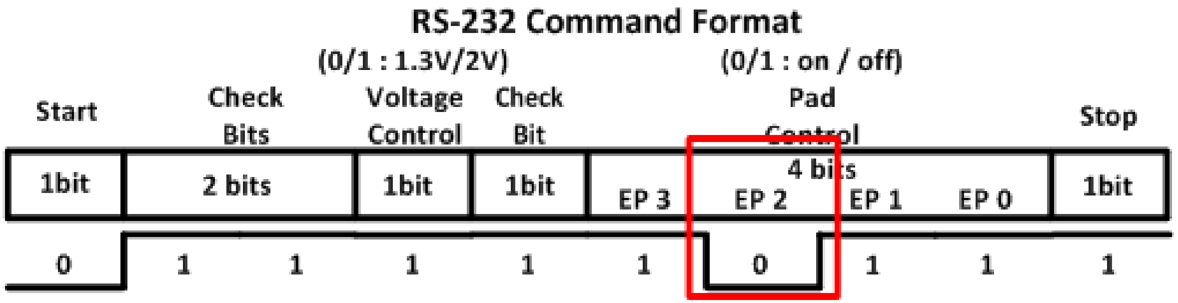
Measured Supply Voltage VDD and Demodulated Command DO

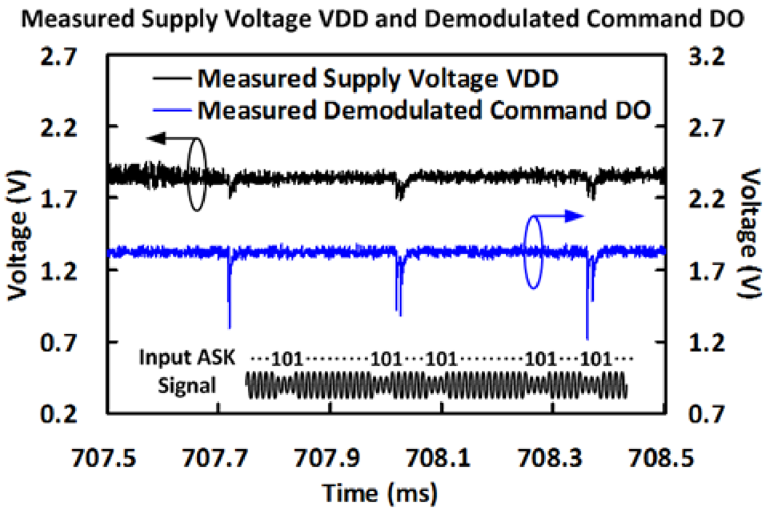


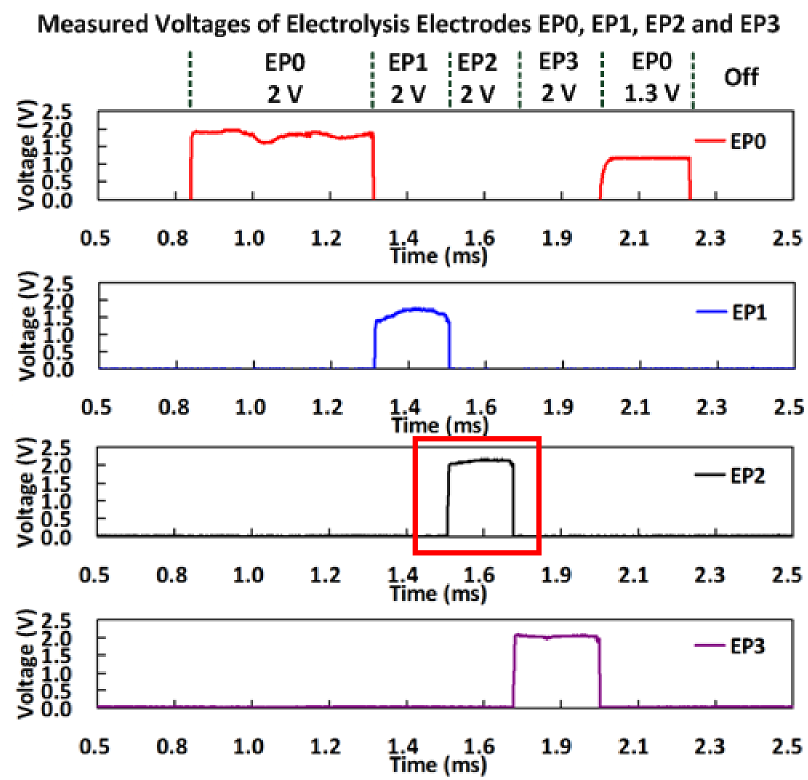
Measured Voltages of Electrolysis Electrodes EP0, EP1, EP2 and EP3



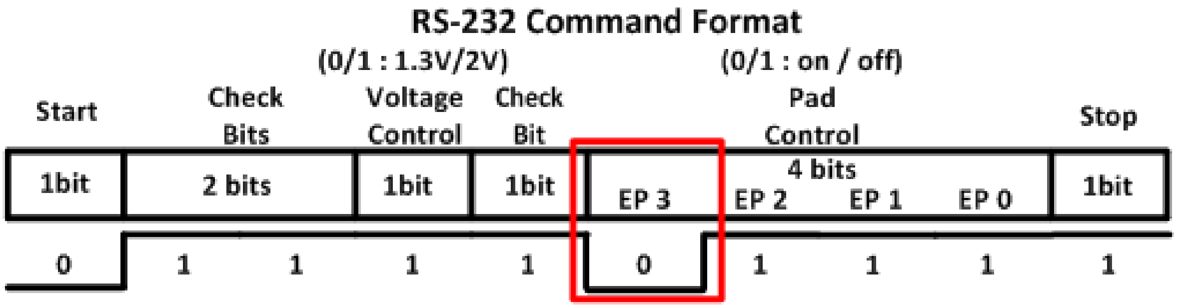
Demodulation

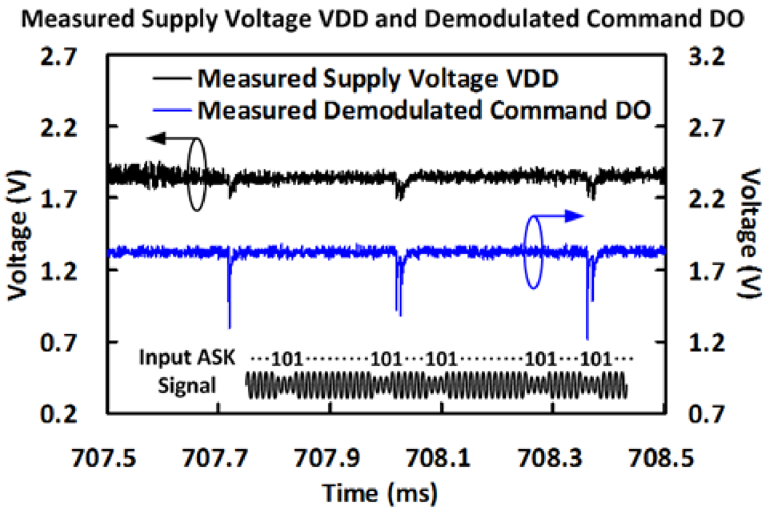


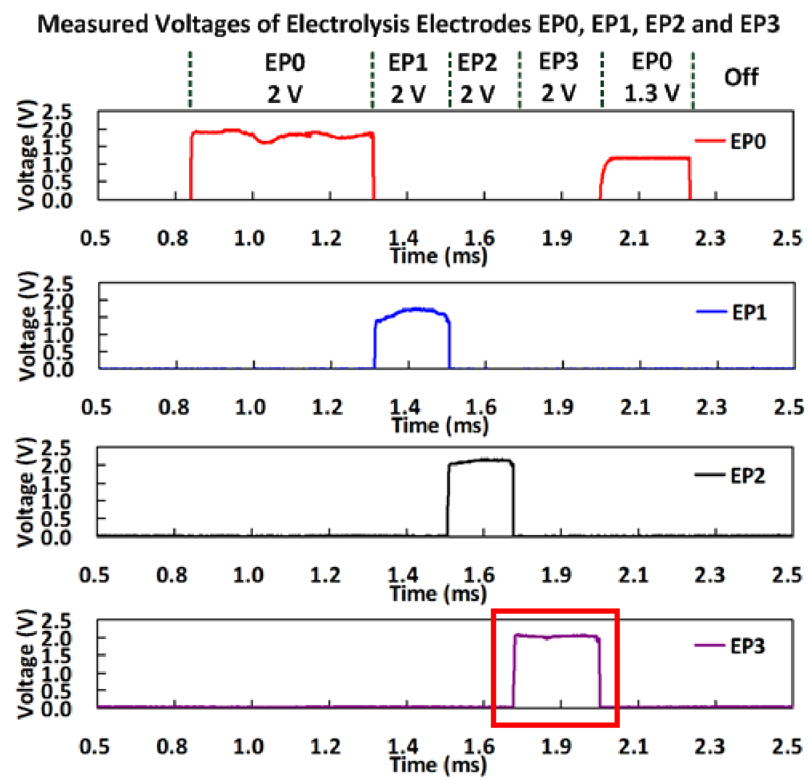




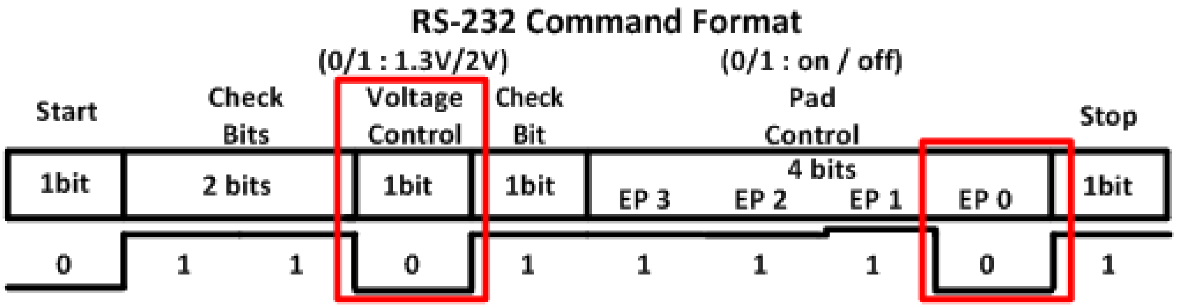
Demodulation

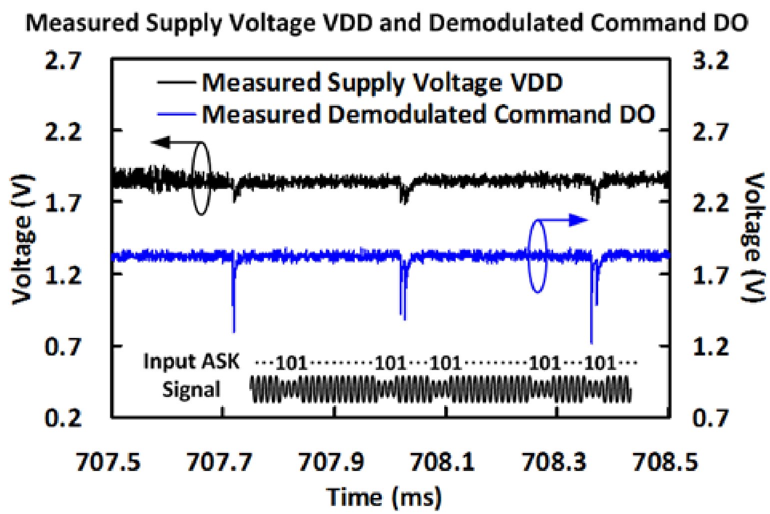


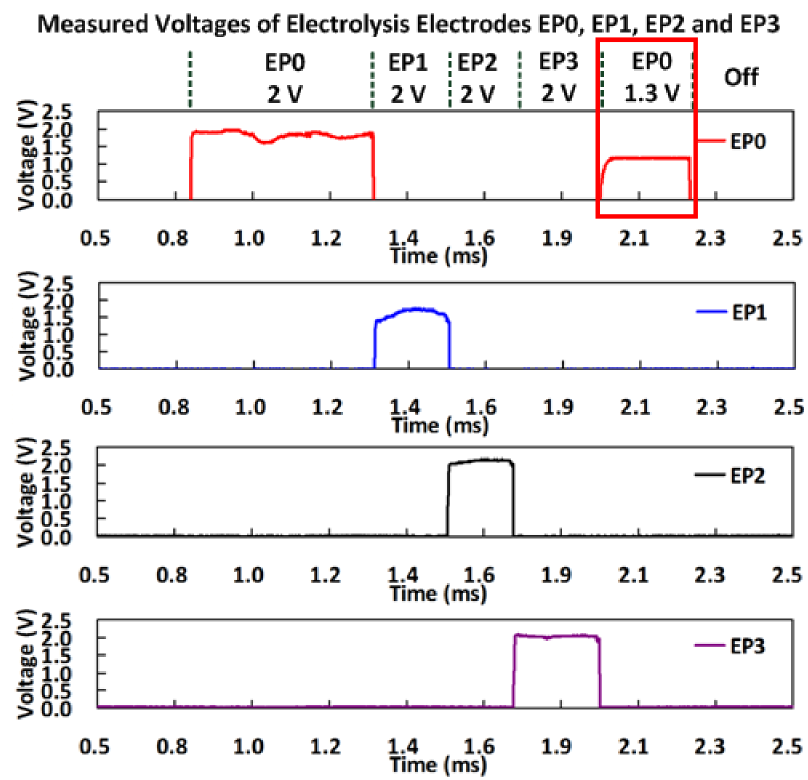




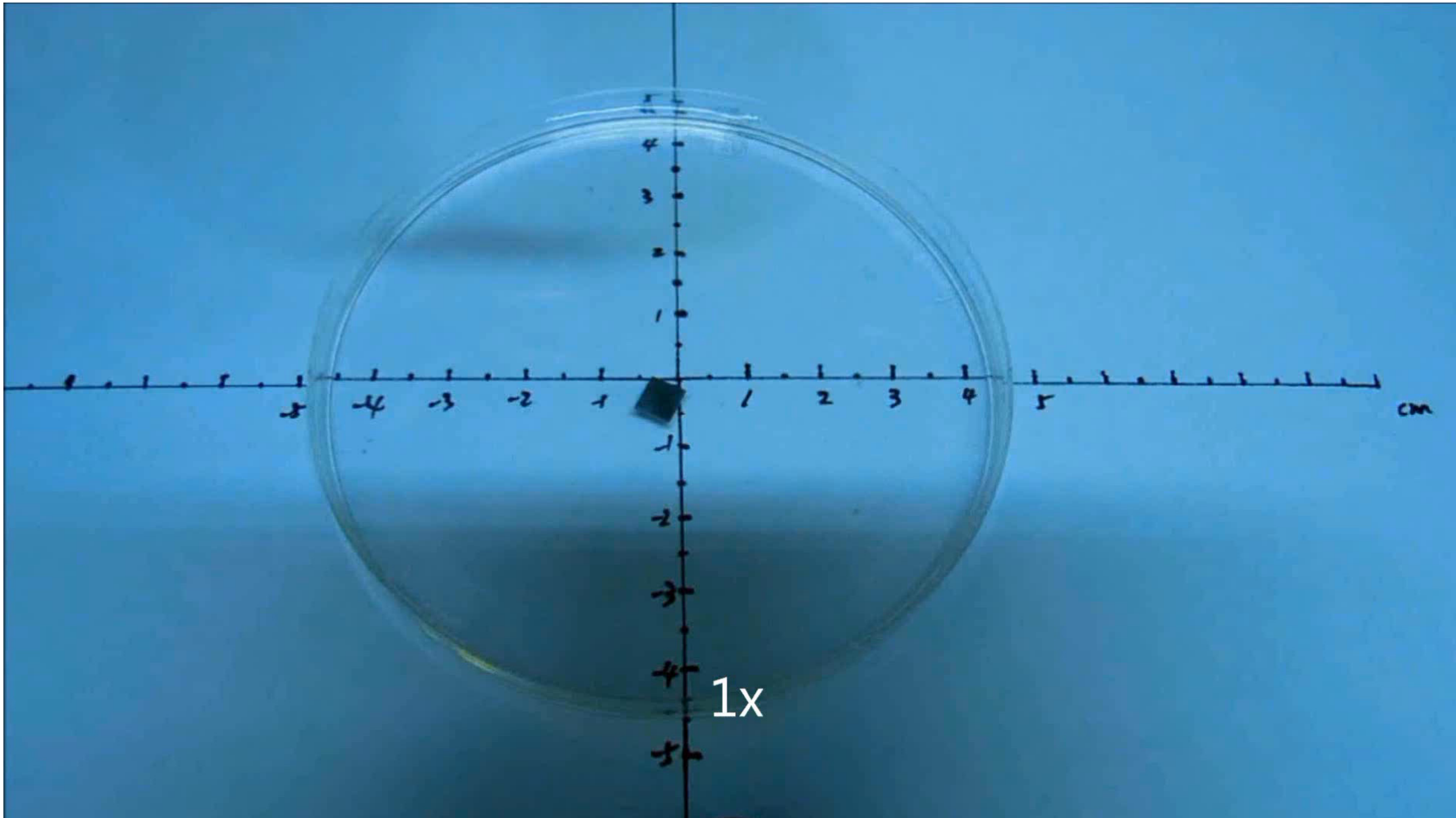
Demodulation







Demo Video



Demo Video2 (Changing Direction)

High flexibility of chip motion.

Performance Summary

	This Work	ISSCC 2012 [2]
Technology	0.35µm CMOS	65nm CMOS
Battery	No	No
Propulsive Force Type	Electrolytic Bubbles	Lorentz Force*
Regulated Voltage	2V (VDD)	0.7V
Modulation Type	ASK	ASK+PWM
RF Carrier Frequency	10MHz	1.86GHz
Command Rate	1Mbps	2.5 - 25Mbps
Power Consumption	125.4µW (Chip Circuit) 82µW (Electrolysis)	17µW (Chip Circuit) 250µW (Fluid Propulsion System)
Chip Size	4.6mm x 4.6mm (including on-chip coils, electrolysis electrodes)	2mm x 2mm (Receive Antenna) 0.6mm x 1mm (Die)
External Component	No	Yes (PCB, Antenna, Magnet)
Electrolytic Voltage	EV2=2V EV1=1.3V	N/A
Moving Directions	4 directions	N/A
Moving Speed	~0.3mm/sec	~0.53cm/sec

* External magnet is required.

Conclusions

- A locomotive SoC is proposed and realized by 0.35μm CMOS technology without any external components.
- Electrolytic bubbles are used for generating reaction force to propel chip.
- Experimental result shows flexibility of direction change.
- In the future, by optimizing electrodes and adaptive driver, moving speed can be improved 100X expectantly.

Acknowledgement

- *Thank the National Chip Implementation Center (CIC) and TSMC for the chip fabrication.*
- *Financial support for this work was provided in part by the National Science Council, Taiwan.*